100GBASE-LR4 CFP2 10km Optical Transceiver
GF2-S101-LR4C/ GF2-S111-LR4C

Features

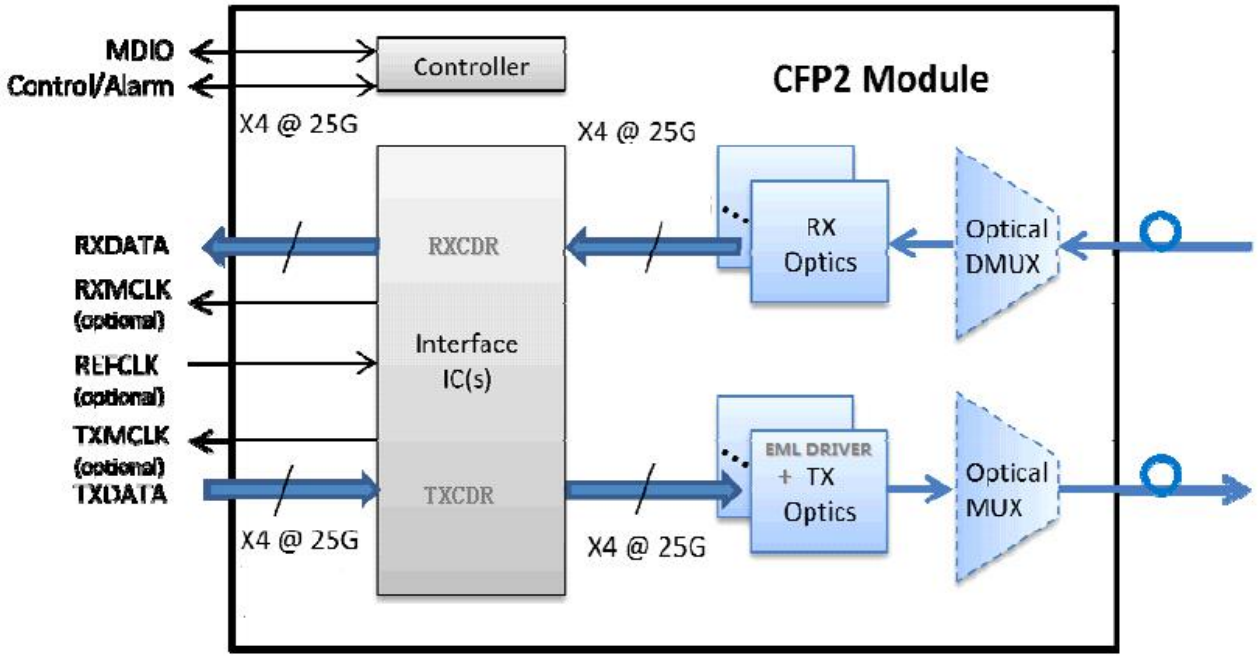
- ✓ 1310 nm window cooled EA-DFB LD and PIN ROSA
- ✓ Operating optical data rate up to 112Gbps
- ✓ CFP2 MSA compliant
- ✓ Compliant to IEEE 802.3ba specification for 100GBASE-LR4
- ✓ Compliant to OTU4
- ✓ Transmission distance up to 10km
- ✓ Operating electrical serial data rate up to 27.952493Gbps
- ✓ 4 parallel electrical serial interface and AC coupling of CML signals
- ✓ MDIO real-time digital diagnostic and control capabilities
- ✓ TX input and RX output CDR retiming
- ✓ Hot pluggable
- ✓ Total Power Consumption<6W
- ✓ Operating case temperature 0°C to +70°C
- ✓ 3.3V power supply
- ✓ Duplex LC receptacle optical interface
- ✓ Compliant with CFP2 MSA hardware specification
- ✓ Compliant with CFP MSA management specification
- ✓ RoHS 2.0 compliant (lead free)

Applications

- ✓ 100GbE IEEE 802.3ba 100GBASE-LR4
- ✓ OTN-OTU4, G.959.1-201604, 4I1-9D1F OTL4.4
- ✓ Switch to switch interface or Switch to router interface

Description

The Gigalight CFP2 100GEBASE-LR4 optical transceiver is a hot pluggable 100Gbps small-form-factor transceiver module .It is compliant with IEEE802.3ba and CFP2 MSA. The module is a multi-rate optical transceiver and intended to support Telecom and Datacom applications.



100GE CFP2 LR4 Module Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{cc}	-0.3	3.6	V
Input Voltage	V_{in}	-0.3	V_{cc}+0.3	V
Storage Temperature	T_s	-20	85	ºC
Case Operating Temperature	T_c	0	70	ºC
Humidity (non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	V_{cc}	3.13	3.3	3.47	V
Operating Case Temperature	T_c	0		70	ºC
Data Rate Per Lane	fd		25.78125	28.05	Gb/s
Humidity	Rh	5		85	%
Power Dissipation	P_m			6	W

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential Input Impedance	Z_{in}	90	100	110	ohm
Differential Output Impedance	Z_{out}	90	100	110	ohm
Differential Input Voltage Amplitude[1]	ΔV_{in}	300		1100	mVp-p
Differential Output Voltage Amplitude[2]	ΔV_{out}	500		800	mVp-p
Skew	Sw			300	ps
Input Logic Level High	V_{IH}	2.0		V_{cc}	V
Input Logic Level Low	V_{IL}	0		0.8	V
Output Logic Level High	V_{OH}	V_{cc}-0.5		V_{cc}	V
Output Logic Level Low	V_{OL}	0		0.4	V

Note:

1. Differential input voltage amplitude is measured between TxnP and TxnN.
2. Differential output voltage amplitude is measured between RxnP and RxnN.

Optical Characteristics （Top=0~70℃，VCC=3.13to3.46 Volts）

Parameter	Symbol	Unit	Value		
			Min	Typ	Max
Optical Transmitter Characteristics					
Signaling Rate for Each Lane (100GbE)	-	Gbps		25.78125	
Signaling Rate for Each Lane (OTU4)				27.9525	
Four lane Wavelength Range	入 1	nm	1294.53	1295.56	1296.59
	入 2		1299.02	1300.05	1301.09
	入 3		1303.54	1304.58	1305.63
	入 4		1308.09	1309.14	1310.19
Average Launch Power for Each Lane(100GbE)	Pa	dBm	-4.3		+4.5
Average Launch Power for Each Lane(OTU4)			-2.5		+4.5
Extinction Ratio (100GbE)	EX	dB	7		
Extinction Ratio (OTU4)			7		
Optical Receiver Characteristics					
Receiver Sensitivity in OMA for Each Lane(100GbE)	Sen	dBm	-	-	-8.6(1)
Receiver Sensitivity for Each Lane(OTU4)					-10.3(2)
Los Assert		dBm			-15
Los De-assert		dBm	-19		
Los Hysteresis		dB		1	2

Notes

（1）Measured with 25.78125Gbps，PRBS 231-1，BER<1E-12

（2）Measured with 27.95Gbps，PRBS 231-1，BER<1E-12

Electrical Characteristics

(Tested under recommended operating conditions, unless otherwise noted)

Parameter	Symbol	Unit	Min	Typ	Max	Note
Receiver						
Differential Data Output Swing	Vout,pp	mV	400	-	800	
Differential Signal Output Resistance		Ω	80	-	120	
Differential Signal Input Resistance		Ω	80	-	120	
LOS Fault	-	V	V_{dd3}-0.5	-	V_{dd3}	
LOS Normal	-	V	0	-	+ 0.5	1
Note1: Vdd3 is host +3.3V power supply.						

Low Speed Electrical Interface

Parameter	Symbol	Unit	Min	Max	Note
Input High Voltage	V_{IH}	V	2.0	V_{cc3} + 0.3	
	V_{IL}	V	-0.3	0.8	
Input Low Voltage	V_{OH}	V	V_{dd3}-0.5	V_{dd3} + 0.3	1
	V_{OL}	V	0.0	0.4	
Input Leakage Current	VIH	V	V_{dd3}*0.7	V_{dd3} + 0.5	1
	VIL	V	-0.3	V_{dd3}*0.3	
Output High Voltage (IOH = 100uA)	VOH	V	V_{dd3}-0.5	V_{dd3} + 0.3	
	VOL	V	0.0	0.4	
Output low Voltage (IOH = 100uA)	IL	uA	-10	10	
Minimum Pulse Width of Control Pin Signal		KHz		400	
1.2V LVCMOS Electrical Characteristics					
Input High Voltage	1.2VIH	V	0.84	1.5	
Input Low Voltage	1.2VIL	V	-0.3	0.36	
Input Leakage Current	1.2IIN	uA	-100	+ 100	
Output High Voltage	1.2V0H	V	1.0	1.5	

Output Low Voltage	1.2V0L	V	-0.3	0.2	
Output High Current	1.2I0H	mA		-4	
Output Low Current	1.2I0L	mA	+4		
Input Capacitance	Ci	pF		10	

Hardware Control Pins

The CFP2 Module support real-time control functions via hardware pins, listed in the following table:

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
17	PRG_CNTL1	Programmable Control 1 MSA Default: RSTn	I	3.3V LVCMOS	per CFP2 MSA Management Interface Specification		Pull-Up Note1
18	PRG_CNTL2	Programmable Control 2 MSA Default : Hardware Interlock LSB	I	3.3V LVCMOS			Pull-Up Note1
19	PRG_CNTL3	Programmable Control 3 MSA Default:Hardware Interlock MSB	I	3.3V LVCMOS			Pull-Up Note1
26	M0D_L0PWR	Module Low Power Mode	I	3.3V LVCMOS	Low Power	Enable	Pull-Up Note1
28	M0D_RSTn	Module Reset(Invert)	I	3.3V LVCMOS	Enable	Reset	Pull-Down Note2
24	TX_DIS	Transmitter Disable	I	3.3V LVCMOS	Disable	Enable	Pull-Up Note1

Note1: Pull-Up resistor (4.7KOhm to 10 K Ohm) is located within the CFP2 module

Note2: Pull-Down resistor (4.7KOhm to 10 k Ohm) is located within the CFP2 module

Hardware Alarm Pins

The CFP2 Module supports alarm hardware pins listed in the following table:

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
20	PRG_ALRM1	Programmable Alarm 1 MSA Default:HIPWR_0N	O	3.3V LVCMOS			
21	PRG_ALRM2	Programmable Alarm 2 MSA Default: MOD_READY	O	3.3V LVCMOS			

22	PRG_ALRM3	Programmable Alarm 3 MSA Default: MOD_FAULT	O	3.3V LVCMOS			
27	MOD_ABS	Module Absent	O	3.3V LVCMOS			Pull-Down Note1
25	RX_LOS	Receiver Loss of Signal	O	3.3V LVCMOS	Loss of Signal	OK	

Note1: Pull-Down resistor (<100ohm) is located within the CFP2 module. Pull-up should be located on the host

Management Interface Pins(MDIO)

The CFP2 Module supports alarm, control and monitor functions via an MDIO bus. The CFP2 MDIO pins are listed in the following table:

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
29	GLB_ALRMn	Global Alarm	I	3.3V LVCMOS	Ok	Alarm	
32	MDIO	Management Data Input Output Bi-Directional Data	I/0	1.2V LVCMOS			
31	MDC	MDIO Clock	I	1.2V LVCMOS			
33	PRTADR0	MDIO Physical Port address bit0	I	1.2V LVCMOS	Per MDIO document		
34	PRTADR1	MDIO Physical Port address bit1	I	1.2V LVCMOS			
35	PRTADR2	MDIO Physical Port address bit2	I	1.2V LVCMOS			

Hardware Signaling Pin Timing Requirements

Timing Parameters for CFP2 hardware Signal Pins are listed in the following table.

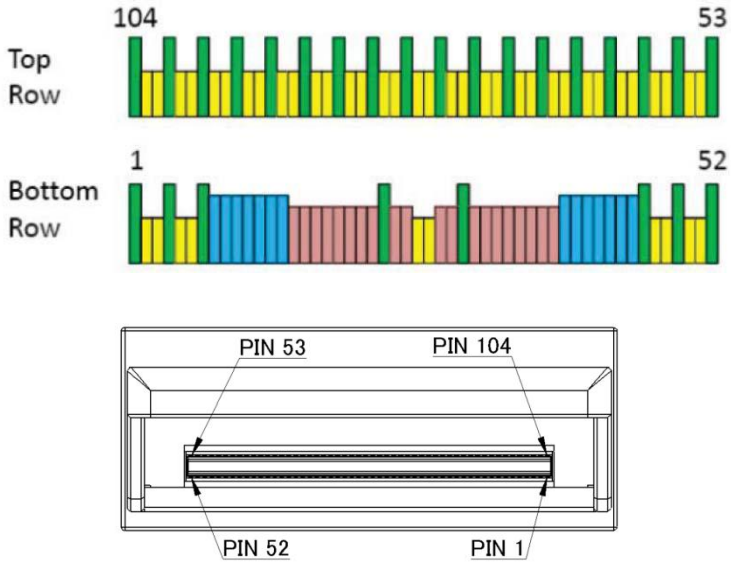
Parameter	Symbol	Min	Max	Unit	Notes&Conditions
Hardware MOD_LOPWR assert	t_MOD_LOPWR_assert		1	ms	Application Specific May depend on current state Condition when signal is applied .See Vendor Datasheet

Hardware MOD_LOPWR deassert	t_MOD_LOPWR_deassert			ms	Value is dependent upon module start-up time.Please See register〞Maximum High-Power-up ime〞in “CFP2 MSA Management Interface Specification”
Receiver Loss of Signal Assert Time	t_loss_assert		100	us	Maximum value designed to support telecom applications
Receiver Loss of Signal De-Assert Time	t_loss_deassert		100	us	Maximum value designed to support telecom applications
Global Alarm Assert Delay Time	GLB_ALRMn_assert		150	ms	This is a logical “OR” of Associated MDIO alarm& status registers.Please see MDIO document for further details
Global Alarm De-assert Delay Time	GLB_ALRMn_deassert		150	ms	This is a logical “OR” of Associated MDIO alarm& status registers.Please see MDIO document for further details
Management Interface Clock Period	t_prd	250		ns	MDC is 4MHz rate
Host MDIO t_setup	t_setup	10		ns	
Host MDIO t_hold	t_hold	10		ns	
CFP2 MDIO t_delay	t_delay	0	175	ns	
Initialization time from Reset	t_initialize		2.5	s	
Transmitter Disabled(TX_DIS_asserted)	t_deassert		100	us	Application Specific
Transmitter Enabled(TX_DIS_asserted)	t_assert		100	ms	Value is dependent upon module start-up time.Please See register “Maximum TX-Turn-on Time” in “CFP2 MSA Management Interface Specification”

Optional Transmitter and Receiver Monitor Clock Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes

Impedance	Zd	80	100	120	Ω	
Frequency			3220		MHz	1/8 of Network lane rate
Output Differential Voltage	VDIFF	400		1200	mV	Peak to Peak Differential
Clock Duty Cycle		40		60	%	



Pad Layout of the CFP2 module

PIN#	Name	I/O	Logic	Description
1	GND			
2	(TX_MCLKn)	O	CML	For optical waveform testing. Not for normal use
3	(TX_MCLKp)	O	CML	For optical waveform testing. Not for normal use
4	GND			
5	N.C.			
6	N.C.			
7	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate,or tied together with Signal Ground
8	3.3V_GND			
9	3.3V			
10	3.3V			
11	3.3V			
12	3.3V			

13	3.3V_GND			
14	3.3V_GND			
15	VND_IO_A	I/O		Module Vendor I/O A. Do Not Connect!
16	VND_IO_B	I/O		Module Vendor I/O B. Do Not Connect!
17	PRG_CNTL1	I	LVCMOS w/ PUR	Programmable Control 1 set over MDIO
18	PRG_CNTL2	I	LVCMOS w/ PUR	Programmable Control 1 set over MDIO
19	PRG_CNTL3	I	LVCMOS w/ PUR	Programmable Control 1 set over MDIO
20	PRG_ALRM1	O	LVCMOS	Programmable Alarm 1 set over MDIO
21	PRG_ALRM2	O	LVCMOS	Programmable Alarm 2 set over MDIO
22	PRG_ALRM3	O	LVCMOS	Programmable Alarm 3 set over MDIO
23	GND			
24	TX_DIS	I	LVCMOS	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0"= transmitter enabled
25	RX_LOS	O	LVCMOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition
26	MOD_LOPWR	I	LVCMOS w/ PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled
27	MOD_ABS	O		Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host
28	MOD_RSTn	I	LVCMOS w/ PDR	Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module
29	GLB_ALRMn	O	LVCMOS	Global Alarm. “0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host
30	GND			
31	MDC	I	1.2V CMOS	Management Data Clock (electrical specs as per 802.3ae and ba)
32	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per 802.3ae and ba)
33	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit 1
34	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit 2
35	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 3
36	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect!
37	VND_IO_D	I/O		Module Vendor I/O D. Do Not Connect!
38	VND_IO_E	I/O		Module Vendor I/O E. Do Not Connect!
39	3.3V_GND			
40	3.3V_GND			

41	3.3V			
42	3.3V			
43	3.3V			
44	3.3V			
45	3.3V_GND			
46	3.3V_GND			
47	N.C.			
48	N.C.			
49	GND			
50	(RX_MCLKn)	O	CML	For optical waveform testing. Not for normal use.
51	(RX_MCLKp)	O	CML	For optical waveform testing. Not for normal use.
52	GND			
53	GND			
54	N.C.			
55	N.C.			
56	GND			
57	RX0p	O	CML	Output Data
58	RX0n	O	CML	Inverted Output Data
59	GND			
60	RX1p	O	CML	Output Data
61	RX1n	O	CML	Inverted Output Data
62	GND			
63	N.C.			
64	N.C.			
65	GND			
66	N.C.			
67	N.C.			
68	GND			
69	RX2P	O	CML	Output Data
70	RX2n	O	CML	Inverted Output Data
71	GND			
72	RX3p	O	CML	Output Data

73	RX3n	O	CML	Inverted Output Data
74	GND			
75	N.C.			
76	N.C.			
77	GND			
78	NC			
79	NC			
80	GND			
81	N.C.			
82	N.C.			
83	GND			
84	TX0p	I	CML	Input Data
85	TX0n	I	CML	Inverted Input Data
86	GND			
87	TX1p	I	CML	Input Data
88	TX1n	I	CML	Inverted Input Data
89	GND			
90	N.C.			
91	N.C.			
92	GND			
93	N.C.			
94	N.C.			
95	GND			
96	TX2p	I	CML	Input Data
97	TX2n	I	CML	Inverted Input Data
98	GND			
99	TX3p	I	CML	Input Data
100	TX3n	I	CML	Inverted Input Data
101	GND			
102	N.C.			
103	N.C.			
104	GND			

Mechanical Dimensions

Unit(MM),General Tolerance:±0.1mm

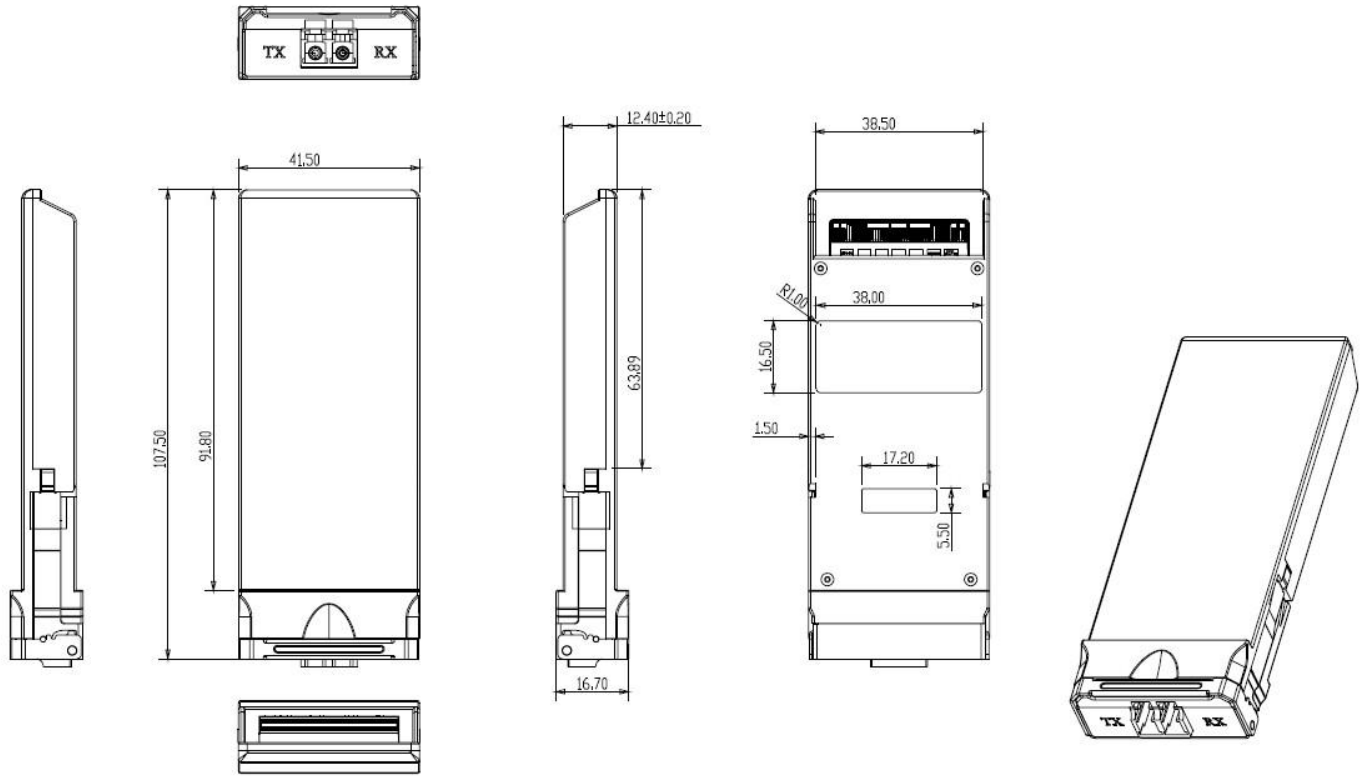


Figure 9. Mechanical Specifications

Regulatory Compliance

Gigalight GF2-S101-LR4C transceivers are Class 1 Laser Products. They are certified per the following standards:

Feature	Standard
Laser Safety	IEC 60825-1:2014 (3rd Edition) IEC 60825-2:2004/AMD2:2010 EN 60825-1-2014 EN 60825-2:2004+A1+A2
Electrical Safety	EN 62368-1: 2014 IEC 62368-1:2014 UL 62368-1:2014
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863
CE EMC	EN55032：2015 EN55035：2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B; ANSI C63.4-2014

⚠CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering Information

Part Number	Product Description
GF2-S101-LR4C	CFP2, 100GE Ethernet,10km, Pout -4.3 ~ +4.5 PIN <-8.6dBm
GF2-S111-LR4C	CFP2, 100GE/OTU4,10km, Pout -2.9 ~ +4.5 PIN <-10.3dBm

Important Notice

Performance figures,data and any illustrative material provided in this data sheet are typical and must be specifically confirmed in writing by Gigalight before they become applicable to any particular order or contract. In accordance with the Gigalight policy of continuous improvement specifications may change without notice.

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Revision History

Revision	Date	Description
V0	Oct-21-2015	Advance Release.
V1	Oct-24-2018	Change the Extinction Ratio (100GbE) 7db to4db Change Total Power Consumption<9W to <6W Add sensitivity test condition

V2	Sep-22-2021	Correct “Hardware Alarm Pins” definition, add pin66~pin69 definition
V3	Jan-19-2022	Revise Tx AOP from -2.9dBm to be -2.5dBm