100G SFP56-DD Active Electrical Loopback Module
GSD-SPO101-LP DSP Version

Features

- ✓ Hot-pluggable SFP-DD form factor
- ✓ 2 channels Electrical Loopback Module
- ✓ Built-in 100G PAM4 DSP
- ✓ Supports 106Gb/s aggregate bit rates
- ✓ Low power dissipation < 2W
- ✓ RoHS compliant and lead free
- ✓ Commercial case temperature range of 0℃ to 70℃
- ✓ Single 3.3V power supply
- ✓ SFP-DD MIS compliant

Applications

- ✓ Board and system level testing
- ✓ Test and measurement
- ✓ Switch and Router chamber testing

Description

Gigalight's GSD-SPO101-LP SFP56-DD active electrical loopback is used for testing 100G SFP56-DD transceiver ports in board level test. By substituting for a full-featured SFP56-DD transceiver, the electrical loopback provides a cost effective low loss method for SFP56-DD port testing.

The GSD-SPO101-LP is packaged in a standard MSA housing compatible with all SFP56-DD ports. Transmit data from the host is electrically routed (internal to the loopback module) to the receive data outputs and back to the host. Since the loopback module does not contain laser diodes, photodiodes, laser driver or transimpedance amplifier chips, etc., it provides an economical way to exercise SFP56-DD ports during R&D validation, production testing and field testing.

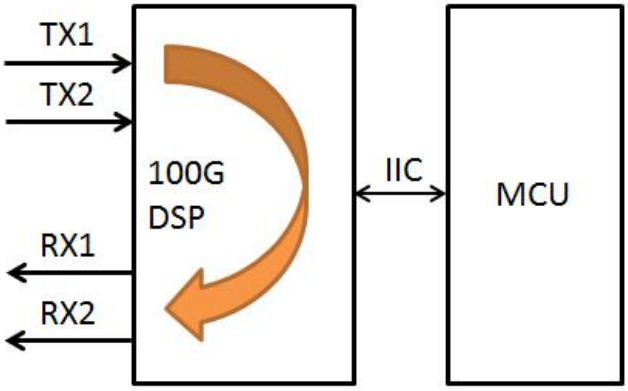

Figure 1. Module Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{cc}	-0.3	3.6	V
Input Voltage	V_{in}	-0.3	V_{cc}+0.3	V
Storage Temperature	T_s	-40	85	℃
Case Operating Temperature	T_c	0	70	℃
Humidity (non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	V_{cc}	3.13	3.3	3.47	V
Operating Case	T_c	0		70	℃
Baud Rate per Lane	fd		26.5625		GBaud/s
Humidity	Rh	5		85	%
Power Dissipation	P_m			2	W

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential Input Impedance	Z_{in}	90	100	110	ohm
Differential Output Impedance	Z_{out}	90	100	110	ohm
Differential Input Voltage Amplitude	ΔV_{in}	300		1100	mVpp
Differential Output Voltage Amplitude	ΔV_{out}	300		900	mVpp
Bit Error Rate	BER			E-12	
Input Logic Level High	V_{IH}	2.0		V_{cc}	V
Input Logic Level Low	V_{IL}	0		0.8	V
Output Logic Level High	V_{OH}	V_{cc}-0.5		V_{cc}	V
Output Logic Level Low	V_{OL}	0		0.4	V

Pin Description

Pin	Logic	Symbol	Name/Description
1		GND	Module Ground Note1
2	LVTTL-O	TXFault	Module Fault Indication: optionally configured as classic SFP Module Fault Indication via TWI as described in the SFP-DD MIS
3	LVTTL-I	TxDisable	Transmitter Disable for classic SFP channel
4	LVCMOS-I/O	SDA	Management I/F data line
5	LVCMOS-I/O	SCL	Management I/F clock
6	LVTTL-O	Mod_ABS	Module Absent
7	LVTTL-I	Speed1	Rx Rate Select for classic SFP channel
8	LVTTL-O	RxLOS	Rx Loss of Signal for classic SFP channe
9	LVTTL-I	Speed2	Tx Rate Select for classic SFP channel
10		GND	Ground Note1
11		GND	Ground Note1
12	CML-O	RD0-	Inverse Received Data Out for classic SFP+ channel
13	CML-O	RD0+	Received Data Out for classic SFP+ channel
14		GND	Ground Note1
15		VccR	Receiver Power Note2
16		VccT	Transmitter Power Note2
17		GND	Ground Note1
18	CML-I	TD0+	Transmit Data In for classic SFP channel
19	CML-I	TD0-	Inverse Transmit Data In for classic SFP channel
20		GND	Ground Note1
21		GND	Ground Note1
22	LVTTL-O	IntL/ TxFaultDD	Interrupt: optionally configured as TxFaultDD via TWI as described in the SFP-DD MIS
23	LVTTL-I	TxDisableDD	Transmitter Disable for DD channel
24	LVTTL-I	ePPS/Clock	Precision Time Protocol (PTP) reference clock input Note3
25	LVTTL-I	LPMode	Low Power Mode Control
26	LVTTL-I	ResetL	Module Reset
27	LVTTL-I	Speed1DD	Rx Rate Select for DD channel
28	LVTTL-O	RxLOSDD	Loss of Signal for DD channel
29	LVTTL-I	Speed2DD	Tx Rate Select for DD channel
30		GND	Ground Note1
31		GND	Ground Note1
32	CML-O	RD1-	Inverse Received Data Out
33	CML-O	RD1+	Received Data Out
34		GND	Ground Note1
35		VccR1	Receiver Power for DD channel Note2
36		VccT1	Transmitter Power for DD channel Note2
37		GND	Ground Note1

38	CML-I	TD1+	Transmit Data
39	CML-I	TD1-	Inverse Transmit Data
40		GND	Ground Note1

Note:

1. SFP-DD uses common ground (GND) for all signals and supply (power). All are common within the SFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signalcommon ground plane.

2. VccR, VccT shall be applied concurrently and VccR1, VccT1 shall be applied concurrently. Requirements defined for the host side of the Host.The connector Vcc pins are each rated for a maximum current of 1000 mA.

3. The ePPS pins (if not used) may be terminated with 50 to ground on the host.

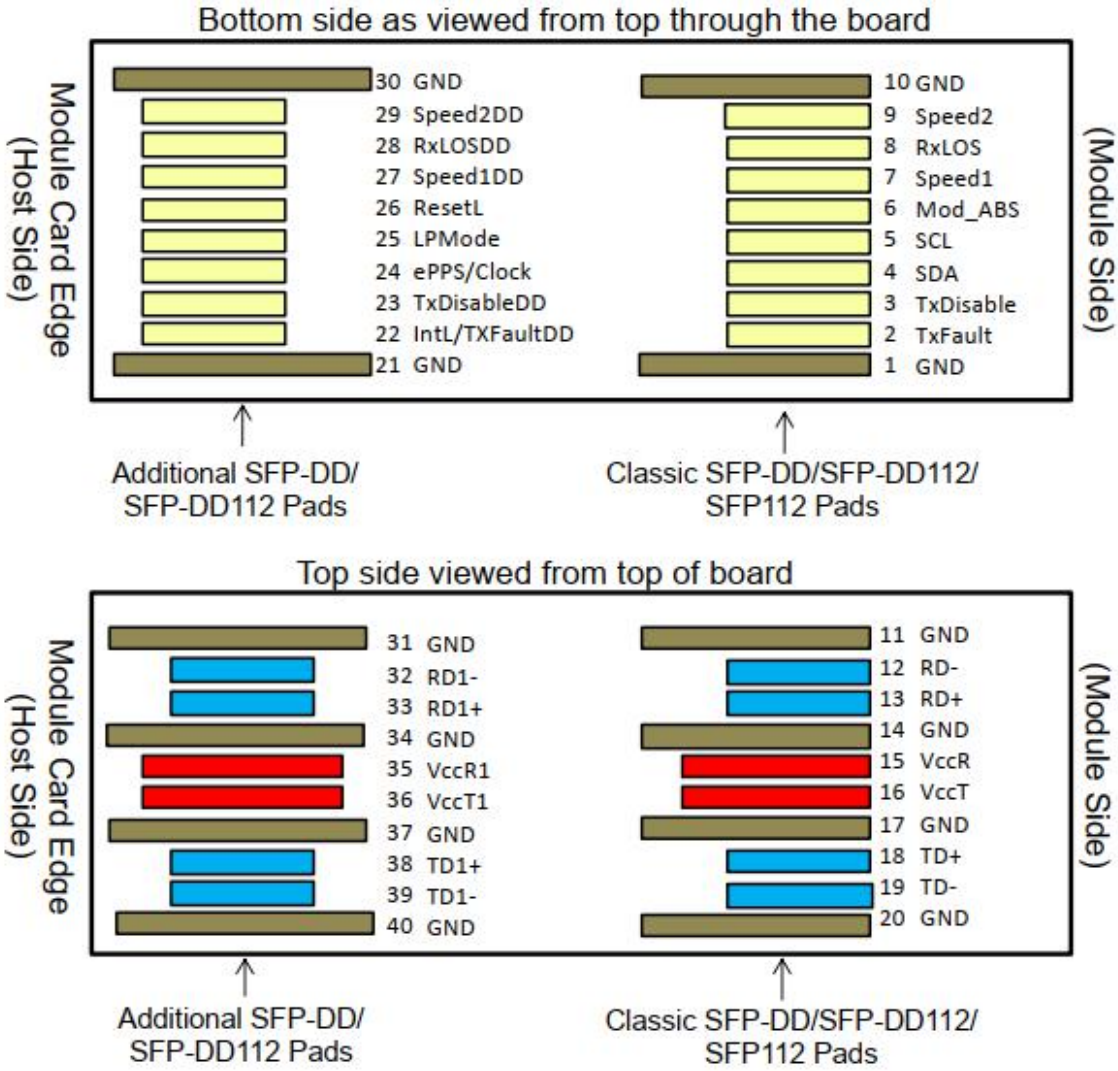

Figure 2. Electrical Pin-out Details

Speed1, Speed2, Speed1DD, Speed2DD

Speed1, Speed2, Speed1DD and Speed2DD are module inputs and are pulled low to GND with >30 k resistors in the module. Speed1 optionally selects the optical receive signaling rate for channel 1. Speed1DD optionally selects the optical receive signaling rate for channel 2. Speed2 optionally selects the optical transmit signaling rate for the channel 1. Speed2DD optionally selects the optical transmit signaling rate for channel 2.

Note: At 128 GFC the FC LSN no longer require to use Speed1, Speed2, Speed1DD and Speed2DD, it is under consideration to reclaim these signals for programmable or other functions.

Mod_ABS

Mod_ABS must be pulled up to Vcc Host on the host board and pulled low in the module. The Mod_ABS is asserted “Low” when the module is inserted. The Mod_ABS is deasserted “High” when the module is physically absent from the host connector due to the pull up resistor on the host board.

LPMode

LPMode is an input signal from the host operating with active high logic. The LPMode signal must be pulled up to Vcc in the SFP-DD/SFP-DD112 module. The LPMode signal allows the host to define whether the SFP- DD/SFP-DD112 module will remain in Low Power Mode until software enables the transition to High Power Mode as defined in the SFP-DD management specification. In Low Power Mode (LPMode de-asserted Low), the module may immediately transition to High Power Mode after the management interface is initialized.

ResetL

The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure 3.

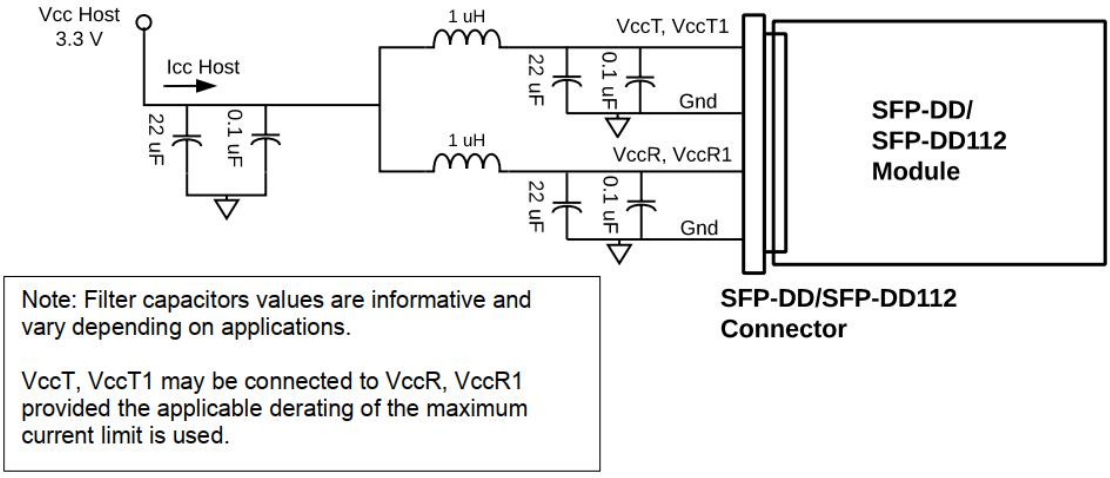

Figure 3. Host Board Power Supply Filtering

DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics functions are available via the I2C interface as specified by SFP-DD MIS. The SFP-DD MIS management memory is shown in Figure 4.

Due to eight-bit addresses, This limits the management memory that can be directly accessed by the host to 256 bytes, which is divided in **Lower Memory** (addresses 00h through 7Fh) and **Upper Memory** (addresses 80h through FFh).

The addressing structure of the additional internal management memory1 is shown in Figure 5. The management memory inside the module is arranged as a unique and always host accessible address space of 128 bytes (Lower Memory) and as multiple upper address subspaces of 128 bytes each (**Pages**), only one of which is selected as host visible in Upper Memory. A second level of Page selection is possible for Pages for which several instances exist (e.g. where a **bank** of pages with the same Page number exists).

This structure supports a flat 256 byte memory for passive copper modules and permits timely access to addresses in the Lower Memory, e.g. Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function in the Lower Page. For more complex modules which require a larger amount of management memory the host needs to use

dynamic mapping of the various Pages into the host addressable Upper Memory address space, whenever needed.

Note: The management memory map has been designed largely after the CMIS memory map where pages and banks are used in order to enable time critical interactions between host and module while expanding the memory size. This memory map has been changed in order to accommodate just two electrical lanes and to limit the required memory. The single address approach is used as found in QSFP.

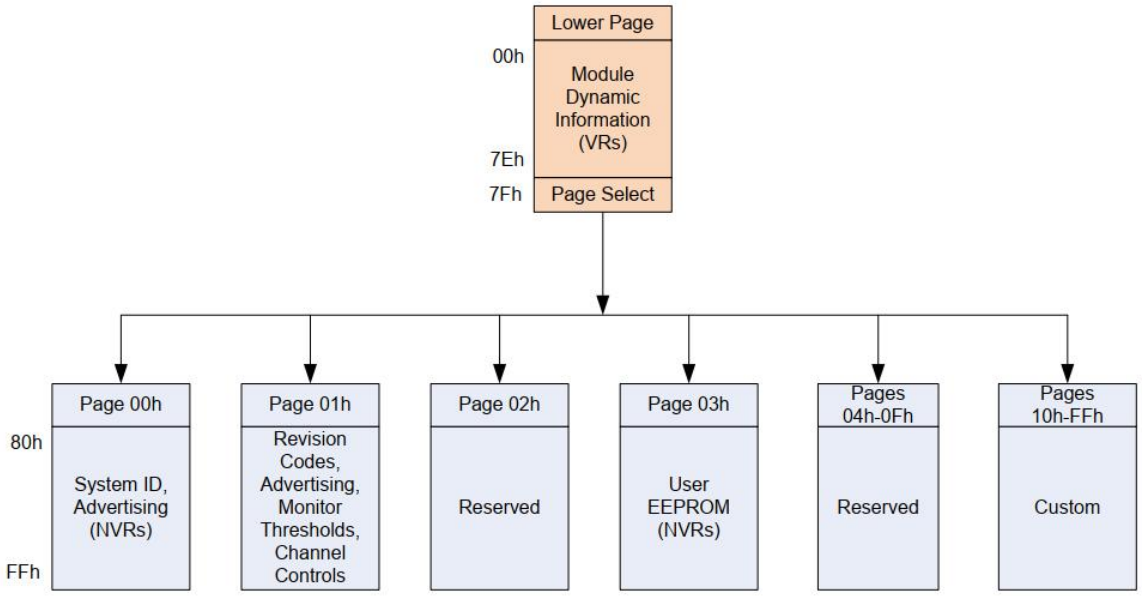

Figure 4. SFP-DD MIS Module Memory Map

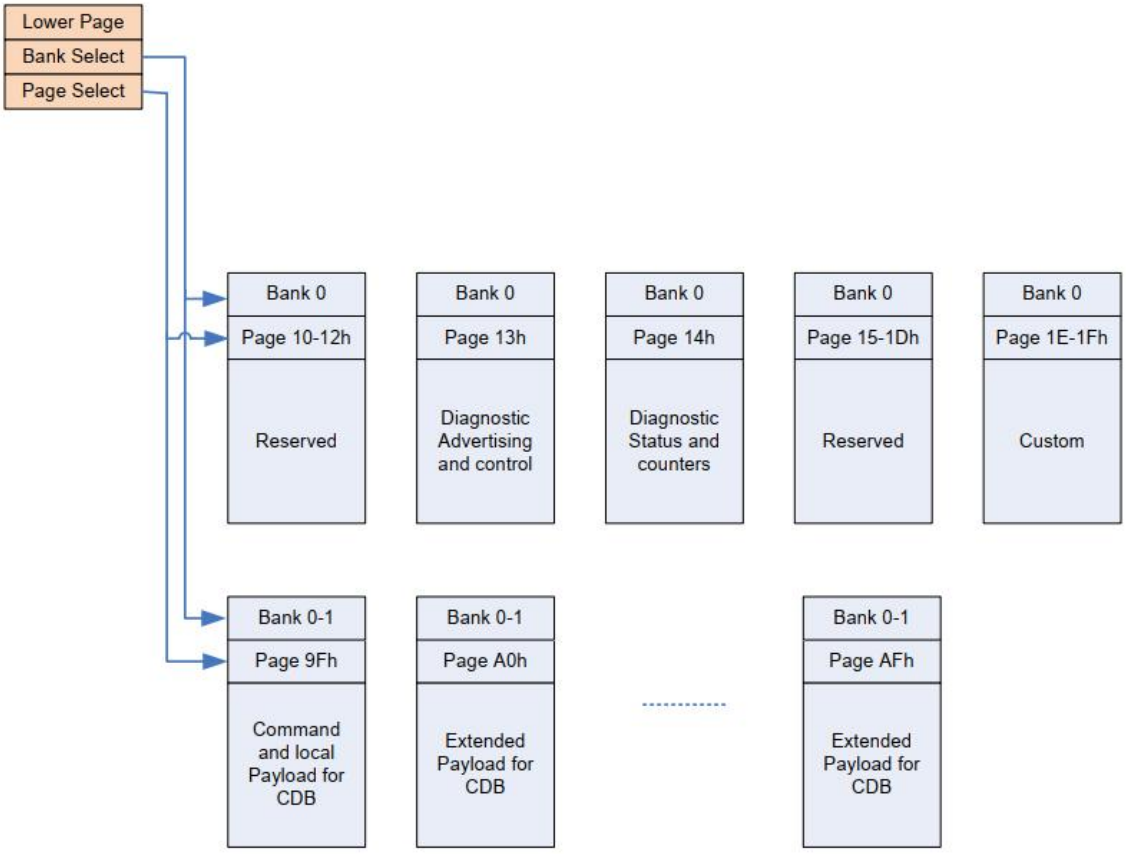

Figure 5. SFP-DD MIS Bank Page Memory Map

The SFP-DD MIS memory also structure allows address space expansion for certain types of modules by allocating additional Pages. Moreover, additional banks of pages can be implemented to support modules with larger management memory needs.

The Lower Memory – Page 00h

The Lower Memory consists of the lower 128 bytes of the 256 byte two-wire serial bus addressable space.

The Lower Page is used to access a variety of module level measurements, diagnostic functions and control functions, as well as to select which of the various Upper Pages in the structured memory map are accessed by byte addresses greater or equal than 128.

This portion of the 256 byte accessible address space is always directly addressable and thus is chosen for monitoring and control functions that may need to be repeatedly accessed.

The lower page is subdivided into several subject areas as shown in the following table.

Address	Size	Subject Area	Description
0–3	4	ID and Status Area	Module ID from SFF-8024 list, version number, Type and status
			Flat mem indication, CLEI present indicator, Maximum TWI speed, Current state of Module, Current state of the Interrupt signal
4-9	6	Lane-Level Flags	Flags that are lane or data path specific
10-13	4	Module-Level Flags	All flags that are not lane or data path specific
14-21	12	Module-Level Monitors	Monitors that are not lane or data path specific
22-25	4	Wavelength and Fiber mapping	
26	1	Module Global Controls	Controls applicable to the module as a whole
27-28	2	Reserved	
29-30	2	Custom	
31-36	6	Reserved	
37-38	2	CDB Status Area	Status of most recent CDB command
39-40	2	Module Firmware Version	Module Firmware Version.
41-52	12	Reserved Area	Reserved for future standardization
53-57	5	Lane Masks	Vendor or module type specific use
58-61	4	Module Masks	
62-73	12	Tx/Rx Power/Bias	
74-82	9	Control Set	
83-84	2	Reserved	
85-117	33	Application Advertising	Combinations of host and media interfaces that are supported by module data path(s)
118-125	8	Password Entry and Change	
126	1	Bank Select Byte	Bank address of currently visible Page
127	1	Page Select Byte	Page address of currently visible Page

Figure 6. The Lower Memory Overview

The Upper Memory – Page 00h (Control and Status Essentials)

Upper page 00h contains static read-only module identification information. Upper page 00h shall be implemented for both paged and flat memory implementations and is required for all modules and cable assemblies.

Address	Size (bytes)	Name	Description
128	1	Identifier	Identifier Type of module
129-144	16	Vendor name	Vendor name (ASCII)
145-147	3	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	2	Vendor rev	Revision level for part number provided by vendor (ASCII)
166-181	16	Vendor SN	Vendor Serial Number (ASCII)
182-189	8	Date Code	
190-199	10	CLEI code	Common Language Equipment Identification code
200-201	2	Module power characteristics	
202	1	Cable assembly length	
203	1	Media Connector Type	
204-207	6	Copper Cable Attenuation	
208-209	2	Reserved	
210-211	2	Cable Assembly Lane Information	
212	1	Media Interface Technology	
213-220	8	Reserved	
221	1	Custom	
222	1	Checksum	Includes bytes 128-221
223-255	33	Custom Info NV	

Figure 7. Page 00h Memory Overview

The Upper Memory – Page 01h (Advertising)

Page 01h contains advertising fields and control fields that are unique to active modules and cable assemblies.

The presence of Page 01h is advertised in bit 7 in Page 00h byte 2.

Byte	Size (bytes)	Name	Description
128-131	4	Module Firmware and Hardware revisions	
132-137	6	Supported link length	Supported lengths of various fiber media
138-139	2	Nominal Wavelength	
140-141	2	Wavelength Tolerance	
142-144	3	Implemented Memory Pages and Durations advertising	
145-154	10	Module Characteristics advertising	
155-156	2	Implemented Controls advertising	
157-158	2	Implemented Flags advertising	
159-160	2	Implemented Monitors advertising	
161-162	2	Implemented Signal Integrity Controls advertising	
163-166	4	CDB support advertising	
167-168	2	Additional Durations advertising	
169-175	7	Reserved	
176-190	15	Module Media Lane advertising	
191-222	32	Custom	
233	1	DataPathDeinit	Data Pathcontrol bits for each lane, controls Data Path State machine
234-239	14	Lane-Specific Control	Fields to control lane attributes independent of the Data Path State machine or control sets
240-245	35	Staged Control Set 0	Fields to configure the selected Application Code and signal integrity settings
246-254	35	Staged Control Set 1	Fields to configure the selected Application Code and signal integrity settings
255	1	Checksum	Checksum of bytes 130-232[1]

Note 1: The firmware version bytes 128-129 are excluded from the checksum to allow module implementers to programmatically generate these fields and avoid requiring a memory map update when firmware is updated.

Figure 8. Page 01h Memory Overview

The Upper Memory – Page 13h (Module Diagnostics 1)

Upper memory map pages 13h and 14h are banked pages that contain module diagnostic control and status fields. The presence of Page 13h is conditional on the state of bit 5 in Page 01h byte 142.

Upper page 13h is subdivided into several areas as illustrated in the following table:

Byte	Size (bytes)	Name	Description
128	1	Loopback capabilities	Module advertisement
129	1	General pattern capabilities	Module advertisement
130	1	Diagnostic reporting capabilities	Module advertisement
131	1	Pattern Generation and Checking locations	Module advertisement
132-142	11	Pattern Generation and Checking capabilities	Module advertisement
143	1	Reserved	Reserved for Module advertisement
144-151	8	Pattern Generator, host side	Host controls
152-159	8	Pattern Generator, media side	Host controls
160-167	8	Pattern Checker, host side	Host controls
168-175	8	Pattern Checker, media side	Host controls
176-179	4	General Generator/Checker controls	Host controls
180-183	4	Loopback controls	Host controls
184-195	12	Reserved	
196-205	10	Custom	
206-223	18	Diagnostic flag masks	Page 14h Flags in bytes 132-149
224-255	32	User Pattern	

Figure 9. Page 13h Memory Overview

The Upper Memory – Page 14h (Module Diagnostics 2)

Upper memory map page 14h is a banked page that contain module diagnostic advertising and control fields. The presence of Page 14h is conditional on the state of bit 5 in Page 01h byte 142. Upper page 14h is subdivided into several areas as illustrated in Table.

Byte	Size (bytes)	Name	Description
128	1	Diagnostics Selector	This selects the content of the data in bytes 192-255
129	1	Reserved	
130-131	2	Custom	
132-139	18	Latched Diagnostics Flags	
140-149	10	Reserved	
192-255	64	Error Information Registers	Contents defined by Diagnostics Selector

Figure 10. Page 14h Memory Overview

Mechanical Dimensions

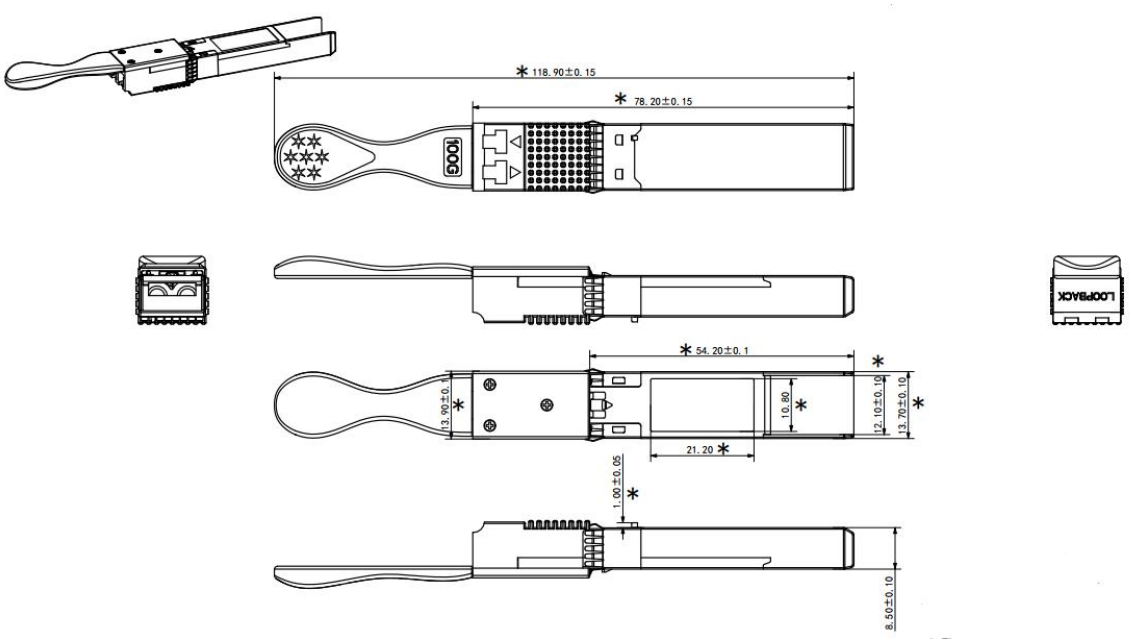

Figure 11. Mechanical Specifications

Regulatory Compliance

Gigalight GSD-SPO101-LP SFP56-DD loopback are Products. They meet the requirements of the following standards.

Feature	Standard
Electrical Safety	EN 62368-1: 2014 IEC 62368-1:2014 UL 62368-1:2014
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863
CE EMC	EN55032：2015 EN55035：2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B ANSI C63.4-2014

References

1. SFP-DD MIS

⚠CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering Information

Part Number	Product Description
GSD-SPO101-LP	100G SFP56-DD Active Electrical Loopback

Important Notice

Performance figures, data and any illustrative material provided in this data sheet are typical and must be specifically confirmed in writing by Gigalight before they become applicable to any particular order or contract. In accordance with the Gigalight policy of continuous improvement specifications may change without notice.

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Revision History

Revision	Date	Description
V0	Aug-3-2023	Advance Release.