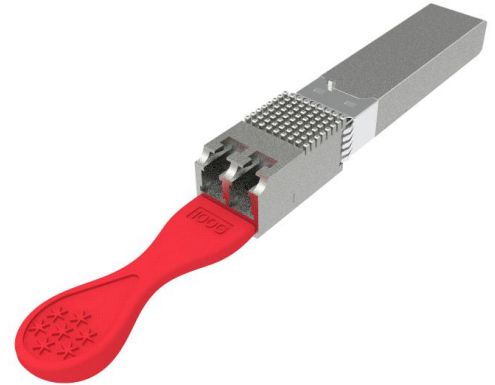


## GIGALIGHT 100G-ER1 Lite -30km SFP56-DD Optical Transceiver

P/N: **GSD-SPO101-ES1CZ**

### Features

- ✓ Compliant to 100G Lambda MSA 100G ER1-30
- ✓ Full-duplex transceiver module
- ✓ 1x106.25Gb/s(PAM4) optical interface
- ✓ 2x53.125Gb/s(PAM4) electrical interface
- ✓ 106.25Gbps PAM4 based on a cooled EML TOSA transmitter
- ✓ 106.25Gbps PAM4 APD Receiver
- ✓ **3.5W** maximum power dissipation
- ✓ Hot-pluggable SFP56-DD form factor
- ✓ Maximum link length of 30km on G.652 SMF with KP-FEC
- ✓ Duplex LC receptacles
- ✓ Built-in digital diagnostic functions
- ✓ Operating case temperature range: 0 to 70°C
- ✓ Single 3.3V power supply
- ✓ RoHS compliant (lead free)



### Applications

- ✓ 100G Lambda 100G ER1-30

### Description

The Gigalight 100G ER1-30km SFP56-DD optical transceiver, 100G SFP56-DD

ER1-30(**GSD-SPO101-ES1CZ**) is designed for using in 100-Gigabit Ethernet links up to 30km over Single-Mode Fiber (SMF). It is compliant with the SFP56-DD MSA, 100G Lambda 100G ER1-30 and CAUI-4(no FEC)<sup>1</sup>. Digital diagnostics functions are available via the I2C interface, as specified by the SFP56-DD MSA.

The module incorporates 1 channel optical signal, on 1311nm center wavelength, operating at 100Gbps data rate. This module can convert 2 channels of 25Gbps (PAM4) electrical input data to 1 channel of 100Gbps (PAM4) optical signal, and also can convert 1 channel of 100Gbps (PAM4) optical signal to 2 channels of 25Gbps (PAM) electrical output data. The optical interface uses a Duplex LC connector. The

high performance cooled EML transmitter and high sensitivity PIN receiver provide superior performance for 100Gigabit Ethernet applications up to 30km links.

**Note:**

1. KR-FEC is optional, please contact us if necessary.

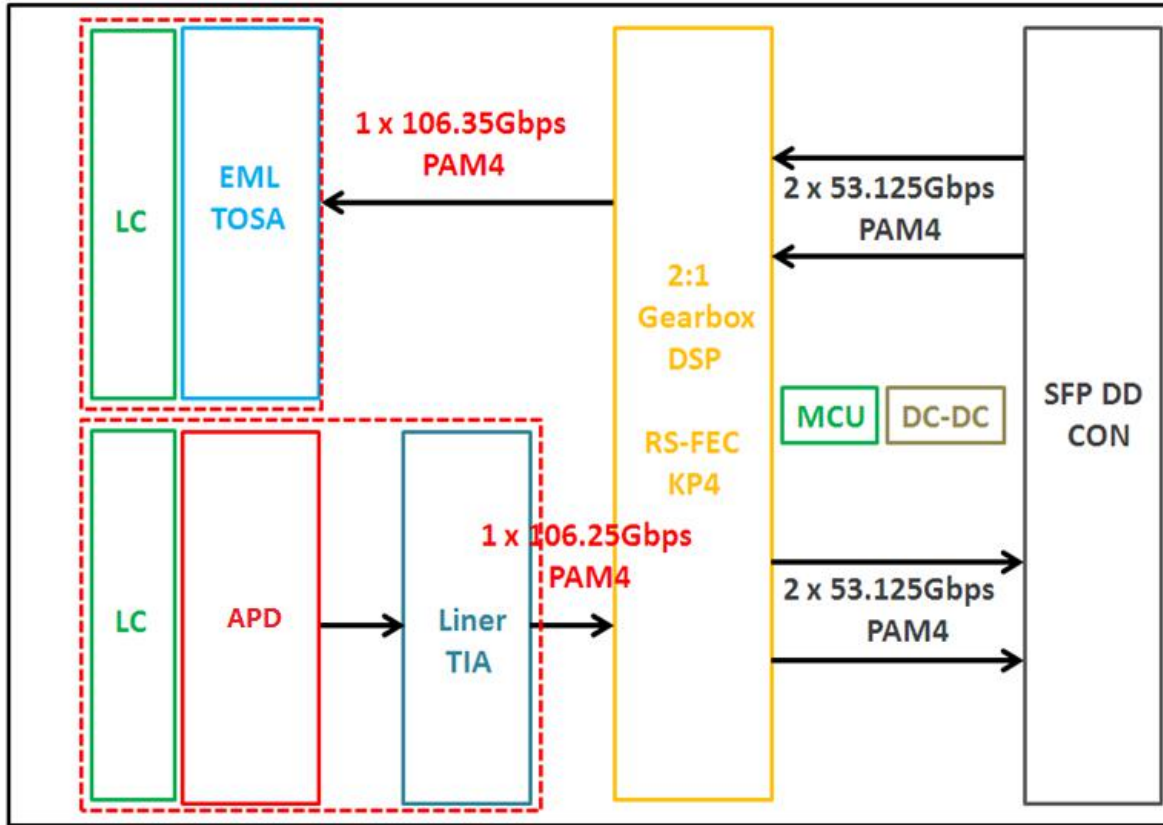


Figure 1. Module Block Diagram

**Absolute Maximum Ratings**

| Parameter                  | Symbol   | Min  | Max          | Unit |
|----------------------------|----------|------|--------------|------|
| Supply Voltage             | $V_{cc}$ | -0.3 | 3.6          | V    |
| Input Voltage              | $V_{in}$ | -0.3 | $V_{cc}+0.3$ | V    |
| Storage Temperature        | $T_s$    | -20  | 85           | °C   |
| Case Operating Temperature | $T_c$    | 0    | 70           | °C   |
| Humidity (non-condensing)  | Rh       | 5    | 85           | %    |

**Recommended Operating Conditions**

| Parameter | Symbol | Min | Typical | Max | Unit |
|-----------|--------|-----|---------|-----|------|
|-----------|--------|-----|---------|-----|------|

|                            |          |      |        |      |      |
|----------------------------|----------|------|--------|------|------|
| Supply Voltage             | $V_{cc}$ | 3.13 | 3.3    | 3.47 | V    |
| Operating Case temperature | $T_c$    | 0    | -      | 70   | °C   |
| Data Rate Per Lane         | $f_d$    | -    | 106.25 | -    | Gb/s |
| Humidity                   | Rh       | 5    | -      | 85   | %    |
| Power Dissipation          | $P_m$    | -    | 3      | 3.5  | W    |
| Link Distance with G.652   | D        | -    | -      | 30   | km   |

### Electrical Specifications

| Parameter  | Symbol           | Min | Typical | Max  | Unit  |
|--|------------------|-----|---------|------|-------|
| Differential Input Impedance                       | $Z_{in}$         | 90  | 100     | 110  | ohm   |
| Differential Output Impedance                      | $Z_{out}$        | 90  | 100     | 110  | ohm   |
| Differential Input Voltage Amplitude <sup>1</sup>  | $\Delta V_{in}$  | -   | -       | 1600 | mVp-p |
| Differential Output Voltage Amplitude <sup>2</sup> | $\Delta V_{out}$ | -   | -       | 900  | mVp-p |

#### Note:

1. Differential input voltage amplitude is measured between TxnP and TxnN.
2. Differential output voltage amplitude is measured between RxnP and RxnN.

### Optical Characteristics

| Parameter                                     | Symbol      | Min    | Typical | Max    | Unit | Notes |
|---|-------------|--------|---------|--------|------|-------|
| <b>Transmitter</b>                            |             |        |         |        |      |       |
| Centre Wavelength                             | $\lambda_c$ | 1304.5 | -       | 1317.5 | nm   | -     |
| Side-mode suppression ratio                   | SMSR        | 30     | -       | -      | dB   | -     |
| Average launch power                          | $P_{out}$   | 0      | -       | 5.6    | dBm  | -     |
| Transmitter and dispersion eye closure(TDECQ) | TDECQ       | -      | -       | 3.9    | dB   | -     |
| Extinction Ratio                              | ER          | 5      | -       | -      | dB   | -     |
| Average launch power of OFF transmitter       |             | -      | -       | -30    | dB   | -     |
| <b>Receiver</b>                               |             |        |         |        |      |       |
| Centre Wavelength                             | $\lambda_c$ | 1304.5 | -       | 1317.5 | nm   | -     |
| Receiver Sensitivity in OMA outer             | $RX_{sen}$  | -      | -       | -12.5  | dBm  | 1     |
| Average receive power                         | $P_{in}$    | -14.7  | -       | -3.4   | dBm  | -     |

|                      |  |     |       |     |     |   |
|----------------------|--|-----|-------|-----|-----|---|
| Receiver Reflectance |  | -   | -     | -26 | dB  | - |
| LOS Assert           |  | -   | -15.7 | -   | dBm | - |
| LOS De-Assert – OMA  |  | -   | -13.7 | -   | dBm | - |
| LOS Hysteresis       |  | 0.5 | -     | -   | dB  | - |
| Damage threshold     |  |     |       | -3  | dBm |   |

**Note:**

1. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FECs

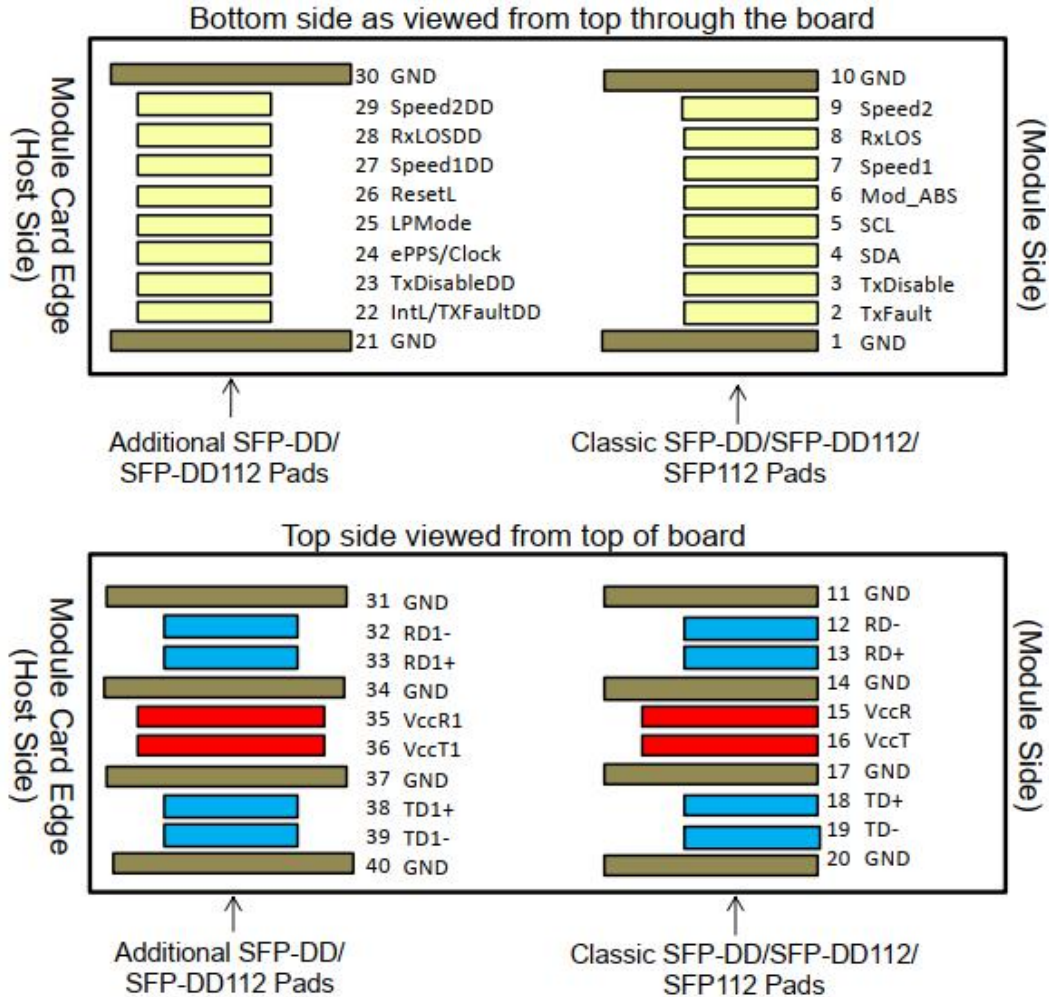
**Pin Description**

| Pin | Logic       | Symbol             | Name/Description   |
|-----|-------------|--------------------|--|
| 1   |             | GND                | Module Ground <sup>Note1</sup>   |
| 2   | LVTTL-O     | TXFault            | Module Fault Indication: optionally configured as classic SFP Module Fault Indication via TWI as |
| 3   | LVTTL-I     | TxDisable          | Transmitter Disable for classic SFP channel  |
| 4   | LVC MOS-I/O | SDA                | Management I/F data line   |
| 5   | LVC MOS-I/O | SCL                | Management I/F clock   |
| 6   | LVTTL-O     | Mod_ABS            | Module Absent  |
| 7   | LVTTL-I     | Speed1             | Rx Rate Select for classic SFP channel   |
| 8   | LVTTL-O     | RxLOS              | Rx Loss of Signal for classic SFP channel  |
| 9   | LVTTL-I     | Speed2             | Tx Rate Select for classic SFP channel   |
| 10  |             | GND                | Ground <sup>Note1</sup>  |
| 11  |             | GND                | Ground <sup>Note1</sup>  |
| 12  | CML-O       | RD0-               | Inverse Received Data Out for classic SFP+ channel   |
| 13  | CML-O       | RD0+               | Received Data Out for classic SFP+ channel   |
| 14  |             | GND                | Ground <sup>Note1</sup>  |
| 15  |             | VccR               | Receiver Power <sup>Note2</sup>  |
| 16  |             | VccT               | Transmitter Power <sup>Note2</sup>   |
| 17  |             | GND                | Ground <sup>Note1</sup>  |
| 18  | CML-I       | TD0+               | Transmit Data In for classic SFP channel   |
| 19  | CML-I       | TD0-               | Inverse Transmit Data In for classic SFP channel   |
| 20  |             | GND                | Ground <sup>Note1</sup>  |
| 21  |             | GND                | Ground <sup>Note1</sup>  |
| 22  | LVTTL-O     | IntL/<br>TxFaultDD | Interrupt: optionally configured as TxFaultDD via TWI as described in the SFP-DD MIS             |

|    |         |             |  |
|----|---------|-------------|--|
| 23 | LVTTL-I | TxDisableDD | Transmitter Disable for DD channel                                   |
| 24 | LVTTL-I | ePPS/Clock  | Precision Time Protocol (PTP) reference clock input <sup>Note3</sup> |
| 25 | LVTTL-I | LPMode      | Low Power Mode Control   |
| 26 | LVTTL-I | ResetL      | Module Reset   |
| 27 | LVTTL-I | Speed1DD    | Rx Rate Select for DD channel  |
| 28 | LVTTL-O | RxLOSDD     | Loss of Signal for DD channel  |
| 29 | LVTTL-I | Speed2DD    | Tx Rate Select for DD channel  |
| 30 |         | GND         | Ground <sup>Note1</sup>  |
| 31 |         | GND         | Ground <sup>Note1</sup>  |
| 32 | CML-O   | RD1-        | Inverse Received Data Out  |
| 33 | CML-O   | RD1+        | Received Data Out  |
| 34 |         | GND         | Ground <sup>Note1</sup>  |
| 35 |         | VccR1       | Receiver Power for DD channel <sup>Note2</sup>                       |
| 36 |         | VccT1       | Transmitter Power for DD channel <sup>Note2</sup>                    |
| 37 |         | GND         | Ground <sup>Note</sup>   |
| 38 | CML-I   | TD1+        | Transmit Dat   |
| 39 | CML-I   | TD1-        | Inverse Transmit Data  |
| 40 |         | GND         | Ground <sup>Note1</sup>  |

**Note:**

1. SFP-DD uses common ground (GND) for all signals and supply (power). All are common within the SFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signalcommon ground plane.
2. VccR, VccT shall be applied concurrently and VccR1, VccT1 shall be applied concurrently. Requirements defined for the host side of the Host.The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. The ePPS pins (if not used) may be terminated with 50 to ground on the host.



**Figure 2. Electrical Pin-out Details**

### Speed1, Speed2, Speed1DD, Speed2DD

Speed1, Speed2, Speed1DD and Speed2DD are module inputs and are pulled low to GND with >30 k resistors in the module. Speed1 optionally selects the optical receive signaling rate for channel 1. Speed1DD optionally selects the optical receive signaling rate for channel 2. Speed2 optionally selects the optical transmit signaling rate for the channel 1. Speed2DD optionally selects the optical transmit signaling rate for channel 2.

Note: At 128 GFC the FC LSN no longer require to use Speed1, Speed2, Speed1DD and Speed2DD, it is under consideration to reclaim these signals for programmable or other functions.

### ResetL Pin

Reset. LPMODE\_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length ( $t_{Reset\_init}$ ) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time ( $t_{init}$ ) starts on the rising edge after the



low level on the ResetL pin is released. During the execution of a reset ( $t_{init}$ ) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data\_Not\_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

### **Mod\_ABS**

Mod\_ABS must be pulled up to Vcc Host on the host board and pulled low in the module. The Mod\_ABS is asserted “Low” when the module is inserted. The Mod\_ABS is deasserted “High” when the module is physically absent from the host connector due to the pull up resistor on the host board.

### **LPMode**

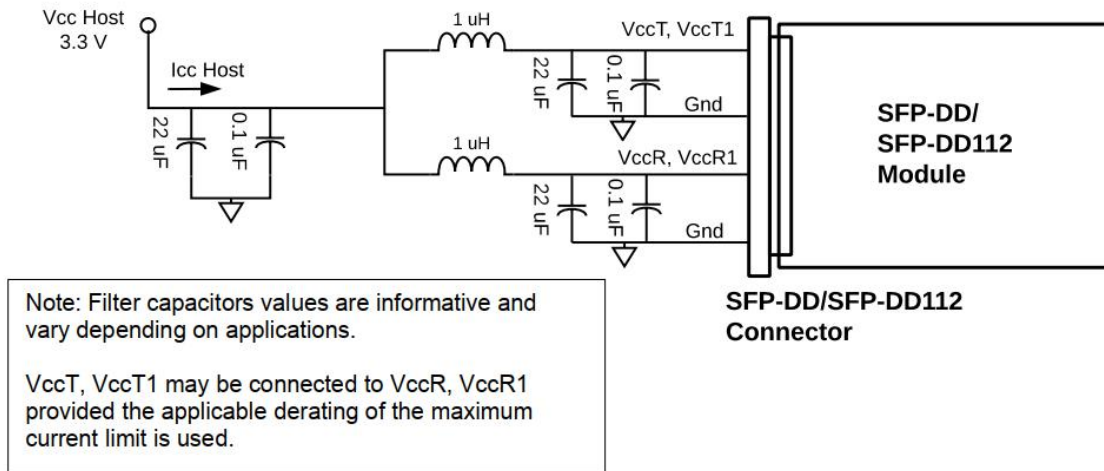
LPMode is an input signal from the host operating with active high logic. The LPMode signal must be pulled up to Vcc in the SFP-DD/SFP-DD112 module. The LPMode signal allows the host to define whether the SFP-DD/SFP-DD112 module will remain in Low Power Mode until software enables the transition to High Power Mode as defined in the SFP-DD management specification. In Low Power Mode (LPMode de-asserted Low), the module may immediately transition to High Power Mode after the management interface is initialized.

### **ResetL**

The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length ( $t_{Reset\_init}$ ) initiates a complete module reset, returning all user module settings to their default state.

### **Power Supply Filtering**

The host board should use the power supply filtering shown in Figure 3.



**Figure 3. Host Board Power Supply Filtering**

### DIAGNOSTIC MONITORING INTERFACE (OPTIONAL)

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

| Parameter                               | Symbol       | Min  | Max | Units | Notes                            |
|---|--------------|------|-----|-------|----------------------------------|
| Temperature monitor absolute error      | DMI_Temp     | -3   | +3  | degC  | Over operating temperature range |
| Supply voltage monitor absolute error   | DMI_VCC      | -0.1 | 0.1 | V     | Over full operating range        |
| Channel RX power monitor absolute error | DMI_RX_Ch    | -2   | 2   | dB    | 1                                |
| Channel Bias current monitor            | DMI_Ibias_Ch | -10% | 10% | mA    |                                  |
| Channel TX power monitor absolute error | DMI_TX_Ch    | -2   | 2   | dB    | 1                                |

**Notes:**

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/- 1 dB fluctuation, or a +/- 3 dB total accuracy.

Digital diagnostics functions are available via the I2C interface as specified by SFP-DD MIS. The SFP-DD MIS management memory is shown in Figure 4.

Due to eight-bit addresses, This limits the management memory that can be directly accessed by the



host to 256 bytes, which is divided in Lower Memory (addresses 00h through 7Fh) and Upper Memory (addresses 80h through FFh).

The addressing structure of the additional internal management memory<sup>1</sup> is shown in Figure 5. The management memory inside the module is arranged as a unique and always host accessible address space of 128 bytes (Lower Memory) and as multiple upper address subspaces of 128 bytes each (Pages), only one of which is selected as host visible in Upper Memory. A second level of Page selection is possible for Pages for which several instances exist (e.g. where a bank of pages with the same Page number exists).

This structure supports a flat 256 byte memory for passive copper modules and permits timely access to addresses in the Lower Memory, e.g. Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function in the Lower Page. For more complex modules which require a larger amount of management memory the host needs to use dynamic mapping of the various Pages into the host addressable Upper Memory address space, whenever needed.

*Note: The management memory map has been designed largely after the CMIS memory map where pages and banks are used in order to enable time critical interactions between host and module while expanding the memory size. This memory map has been changed in order to accommodate just two electrical lanes and to limit the required memory. The single address approach is used as found in QSFP.*

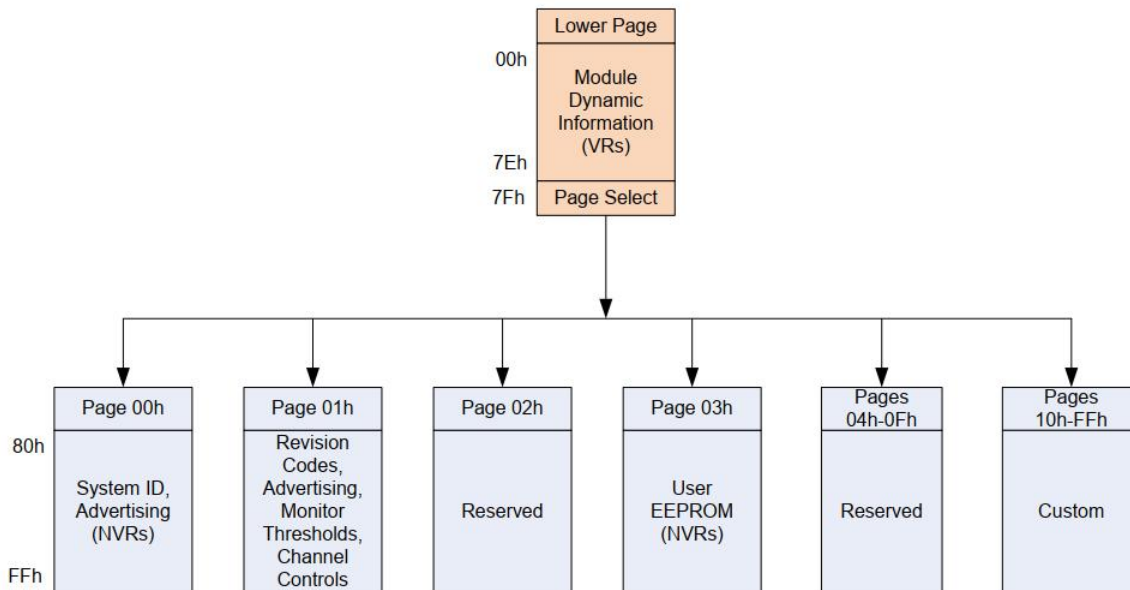


Figure 4. QSFP28 Memory Map

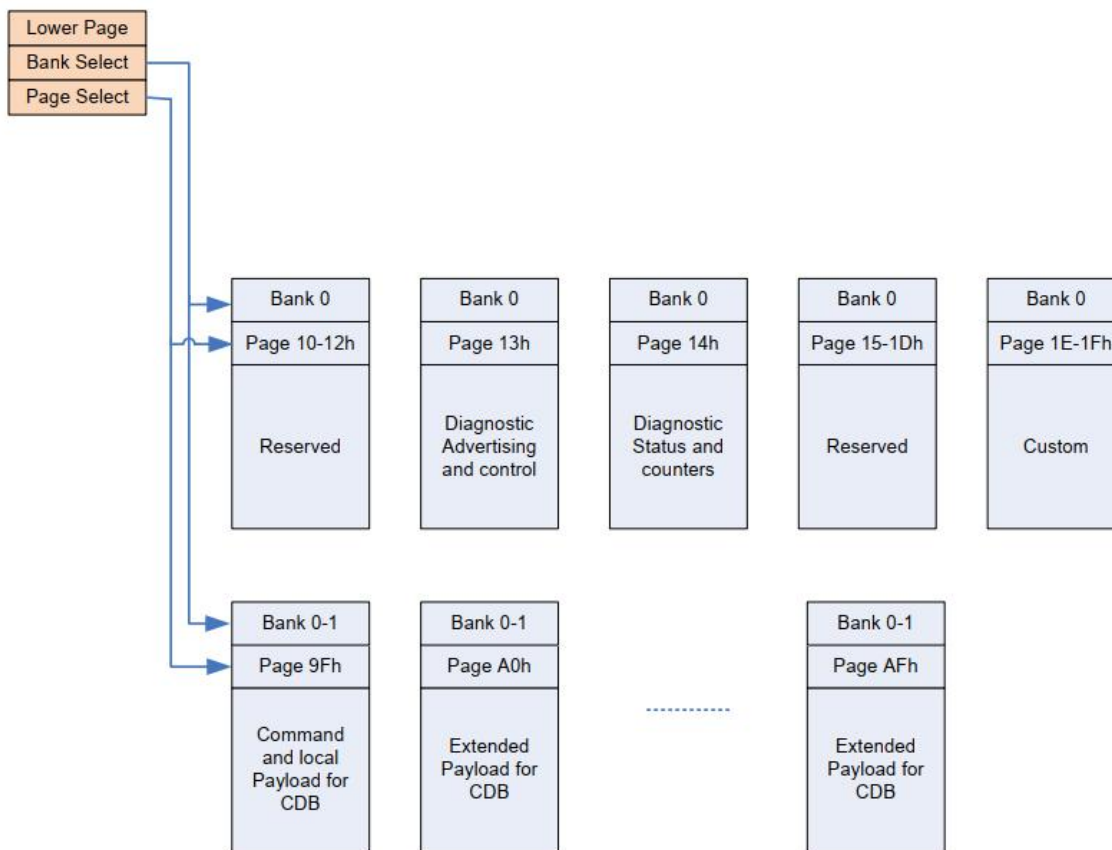


Figure 5. SFP-DD MIS Bank Page Memory Map

| Address | Size | Subject Area                 | Description   |
|---------|------|------------------------------|---|
| 0-3     | 4    | ID and Status Area           | Module ID from SFF-8024 list, version number, Type and status<br>Flat mem indication, CLEI present indicator, Maximum TWI speed, Current state of Module, Current state of the Interrupt signal |
| 4-9     | 6    | Lane-Level Flags             | Flags that are lane or data path specific   |
| 10-13   | 4    | Module-Level Flags           | All flags that are not lane or data path specific   |
| 14-21   | 12   | Module-Level Monitors        | Monitors that are not lane or data path specific  |
| 22-25   | 4    | Wavelength and Fiber mapping |   |
| 26      | 1    | Module Global Controls       | Controls applicable to the module as a whole  |
| 27-28   | 2    | Reserved                     |   |
| 29-30   | 2    | Custom                       |   |
| 31-36   | 6    | Reserved                     |   |
| 37-38   | 2    | CDB Status Area              | Status of most recent CDB command   |
| 39-40   | 2    | Module Firmware Version      | Module Firmware Version.  |
| 41-52   | 12   | Reserved Area                | Reserved for future standardization   |
| 53-57   | 5    | Lane Masks                   | Vendor or module type specific use  |
| 58-61   | 4    | Module Masks                 |   |
| 62-73   | 12   | Tx/Rx Power/Bias             |   |
| 74-82   | 9    | Control Set                  |   |
| 83-84   | 2    | Reserved                     |   |
| 85-117  | 33   | Application Advertising      | Combinations of host and media interfaces that are supported by module data path(s)   |
| 118-125 | 8    | Password Entry and Change    |   |
| 126     | 1    | Bank Select Byte             | Bank address of currently visible Page  |
| 127     | 1    | Page Select Byte             | Page address of currently visible Page  |

**Figure 6. The Lower Memory Overview**

| Address | Size (bytes) | Name                            | Description   |
|---------|--------------|---------------------------------|---|
| 128     | 1            | Identifier                      | Identifier Type of module                                 |
| 129-144 | 16           | Vendor name                     | Vendor name (ASCII)                                       |
| 145-147 | 3            | Vendor OUI                      | Vendor IEEE company ID                                    |
| 148-163 | 16           | Vendor PN                       | Part number provided by vendor (ASCII)                    |
| 164-165 | 2            | Vendor rev                      | Revision level for part number provided by vendor (ASCII) |
| 166-181 | 16           | Vendor SN                       | Vendor Serial Number (ASCII)                              |
| 182-189 | 8            | Date Code                       |   |
| 190-199 | 10           | CLEI code                       | Common Language Equipment Identification code             |
| 200-201 | 2            | Module power characteristics    |   |
| 202     | 1            | Cable assembly length           |   |
| 203     | 1            | Media Connector Type            |   |
| 204-207 | 6            | Copper Cable Attenuation        |   |
| 208-209 | 2            | Reserved                        |   |
| 210-211 | 2            | Cable Assembly Lane Information |   |
| 212     | 1            | Media Interface Technology      |   |
| 213-220 | 8            | Reserved                        |   |
| 221     | 1            | Custom                          |   |
| 222     | 1            | Checksum                        | Includes bytes 128-221                                    |
| 223-255 | 33           | Custom Info NV                  |   |

**Figure 7. Page 00h Memory Overview**

| Byte    | Size (bytes) | Name   | Description  |
|---------|--------------|--|--|
| 128-131 | 4            | Module Firmware and Hardware revisions             |  |
| 132-137 | 6            | Supported link length                              | Supported lengths of various fiber media   |
| 138-139 | 2            | Nominal Wavelength                                 |  |
| 140-141 | 2            | Wavelength Tolerance                               |  |
| 142-144 | 3            | Implemented Memory Pages and Durations advertising |  |
| 145-154 | 10           | Module Characteristics advertising                 |  |
| 155-156 | 2            | Implemented Controls advertising                   |  |
| 157-158 | 2            | Implemented Flags advertising                      |  |
| 159-160 | 2            | Implemented Monitors advertising                   |  |
| 161-162 | 2            | Implemented Signal Integrity Controls advertising  |  |
| 163-166 | 4            | CDB support advertising                            |  |
| 167-168 | 2            | Additional Durations advertising                   |  |
| 169-175 | 7            | Reserved   |  |
| 176-190 | 15           | Module Media Lane advertising                      |  |
| 191-222 | 32           | Custom   |  |
| 233     | 1            | DataPathDeinit                                     | Data Pathcontrol bits for each lane, controls Data Path State machine                        |
| 234-239 | 14           | Lane-Specific Control                              | Fields to control lane attributes independent of the Data Path State machine or control sets |
| 240-245 | 35           | Staged Control Set 0                               | Fields to configure the selected Application Code and signal integrity settings              |
| 246-254 | 35           | Staged Control Set 1                               | Fields to configure the selected Application Code and signal integrity settings              |
| 255     | 1            | Checksum   | Checksum of bytes 130-232 <sup>1</sup>   |

Note 1: The firmware version bytes 128-129 are excluded from the checksum to allow module implementers to programmatically generate these fields and avoid requiring a memory map update when firmware is updated.

**Figure 8. Page 01h Memory Overview**

| Byte    | Size (bytes) | Name   | Description                       |
|---------|--------------|--|-----------------------------------|
| 128     | 1            | Loopback capabilities                        | Module advertisement              |
| 129     | 1            | General pattern capabilities                 | Module advertisement              |
| 130     | 1            | Diagnostic reporting capabilities            | Module advertisement              |
| 131     | 1            | Pattern Generation and Checking locations    | Module advertisement              |
| 132-142 | 11           | Pattern Generation and Checking capabilities | Module advertisement              |
| 143     | 1            | Reserved                                     | Reserved for Module advertisement |
| 144-151 | 8            | Pattern Generator, host side                 | Host controls                     |
| 152-159 | 8            | Pattern Generator, media side                | Host controls                     |
| 160-167 | 8            | Pattern Checker, host side                   | Host controls                     |
| 168-175 | 8            | Pattern Checker, media side                  | Host controls                     |
| 176-179 | 4            | General Generator/Checker controls           | Host controls                     |
| 180-183 | 4            | Loopback controls                            | Host controls                     |
| 184-195 | 12           | Reserved                                     |                                   |
| 196-205 | 10           | Custom                                       |                                   |
| 206-223 | 18           | Diagnostic flag masks                        | Page 14h Flags in bytes 132-149   |
| 224-255 | 32           | User Pattern                                 |                                   |

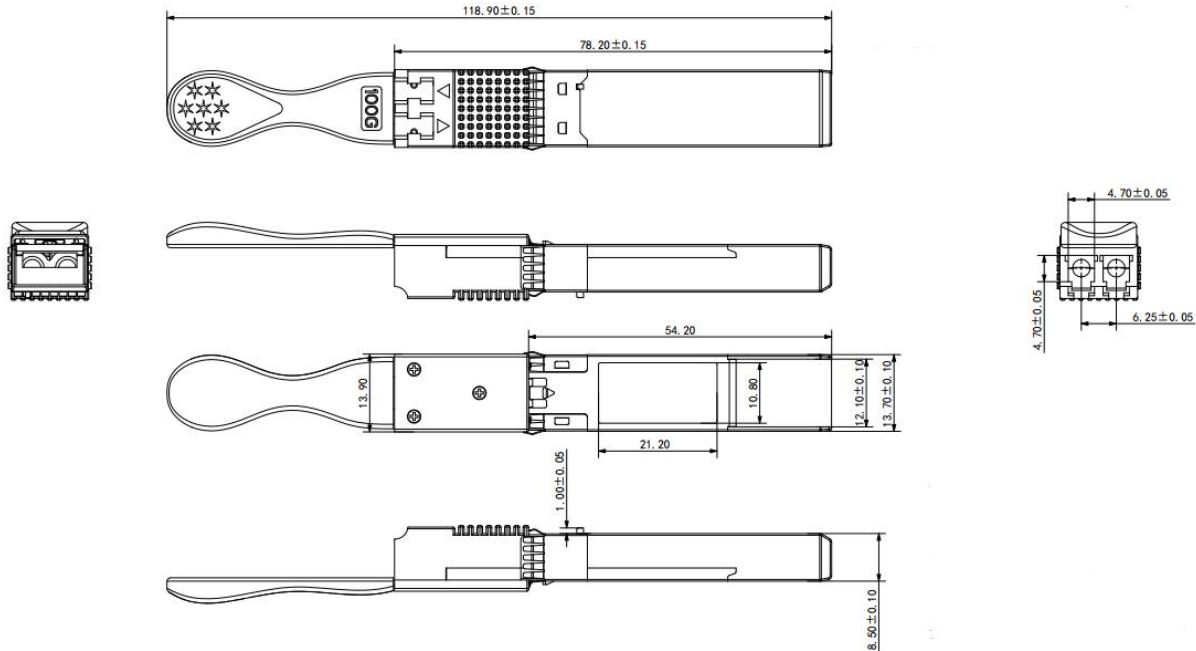
**Figure 9. Page 13h Memory Overview**



| Byte    | Size (bytes) | Name                        | Description   |
|---------|--------------|-----------------------------|---|
| 128     | 1            | Diagnostics Selector        | This selects the content of the data in bytes 192-255 |
| 129     | 1            | Reserved                    |   |
| 130-131 | 2            | Custom                      |   |
| 132-139 | 18           | Latched Diagnostics Flags   |   |
| 140-149 | 10           | Reserved                    |   |
| 192-255 | 64           | Error Information Registers | Contents defined by Diagnostics Selector              |

**Figure 10. Page 14h Memory Overview**

### Mechanical Dimensions



**Figure 8. Mechanical Specifications**

### Regulatory Compliance

Gigalight **GSD-SPO101-ES1CZ** transceivers are Class 1 Laser Products. They meet the requirements of the following standards.

| Feature                  | Standard   |
|--------------------------|--|
| Laser Safety             | IEC 60825-1:2014 (3 <sup>rd</sup> Edition)<br>IEC 60825-2:2004/AMD2:2010<br>EN 60825-1-2014<br>EN 60825-2:2004+A1+A2 |
| Electrical Safety        | EN 62368-1: 2014<br>IEC 62368-1:2014<br>UL 62368-1:2014  |
| Environmental protection | Directive 2011/65/EU with amendment(EU)2015/863  |

|        |  |
|--------|--|
| CE EMC | EN55032: 2015<br>EN55035: 2017<br>EN61000-3-2:2014<br>EN61000-3-3:2013 |
| FCC    | FCC Part 15, Subpart B<br>ANSI C63.4-2014                              |

## References

1. QSFP28 MSA
2. SFF-8436 QSFP+
3. IEEE802.3cu 100GBASE-LR1
4. 100G Lambda MSA **100G ER1-30**

## Ordering Information

| Part Number             | Product Description                                      |
|-------------------------|--|
| <b>GSD-SPO101-ES1CZ</b> | SFP56-DD ER1-30, 106.25Gb/s, 30km, EML+APD, SMF, Dual LC |

### CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

## Important Notice

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## Revision History

| Revision | Date        | Description      |
|----------|-------------|------------------|
| V0       | Aug-01-2023 | Advance Release. |