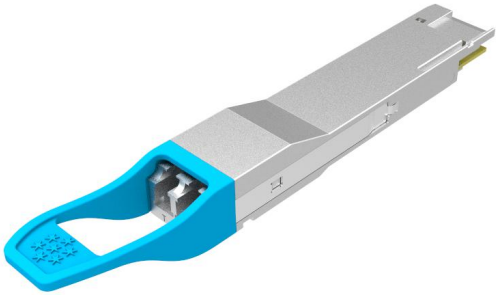
GIGALIGHT 200G QSFP-DD LR4 10km Optical Transceiver Module

GQD-SPO201-LR4CZ



Features

- ✓ 4x53.125Gbps(26.5625GBd) PAM4 LWDM optics architecture
- ✓ 8x25.78125 or 26.5625Gbps Electrical Interface (200GAUI-8)
- ✓ 4x53Gbps PAM4 optical transmitter and receiver
- ✓ 4 channels LWDM cooled EML transmitter
- ✓ 4 channels PIN photo detector array receiver
- ✓ Internal 8:4 Gearbox DSP with KP FEC (optional)
- ✓ Power consumption <9W
- ✓ Hot Pluggable QSFP DD form factor and Compliant with CMIS 4.0
- ✓ Up to 10km transmission over G.652 SMF
- ✓ Duplex LC connector receptacle
- ✓ Built-in digital diagnostic functions
- ✓ Operating case temperature from 0℃ to +70℃
- ✓ 3.3V power supply voltage
- ✓ RoHS compliant (lead free)

Applications

- ✓ 200GBASE-LR4 Ethernet
- ✓ Datacenter

Description

Gigalight's GQD-SPO201-LR4CZ 200GE QSFP-DD Optical Transceiver modules are designed for using in 200Gigabit Ethernet 10km links over SMF single-mode fiber. They are compliant with the QSFP-DD MSA and with IEEE 802.3cn 200GBASE-LR4 specification. Digital diagnostics functions are

available via the I2C interface as specified by CMIS V4.0. These modules can convert 8 channels of 25Gbps (NRZ) electrical input data to 4 channels of 50Gbps (PAM4) optical signal, and also can convert 4 channels of 50Gbps (PAM4) optical signal to 8 channels of 25Gbps (NRZ) electrical output data. And these modules incorporate Gigalight Technologies proven circuit and EML technology to provide reliable long life, high performance, and consistent service.

Note:

1. KP-FEC is optional, please contact us if necessary.

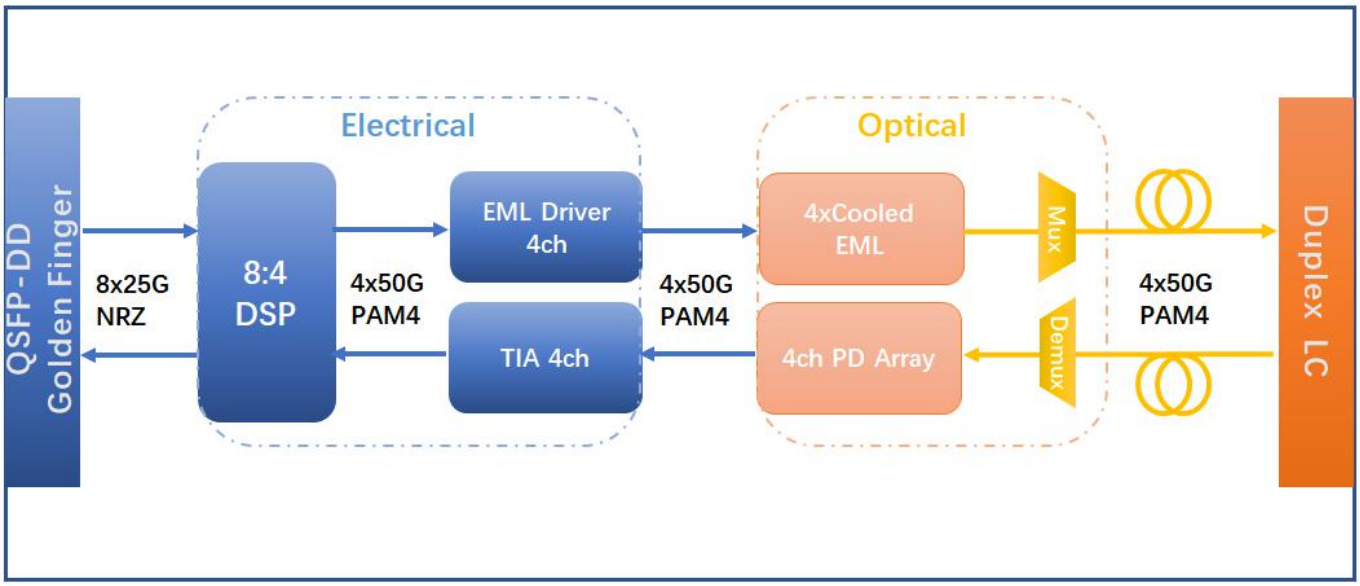


Figure1. Module Block Diagram

200GBASE-LR4 QSFP DD is one kind of LWDM transceiver. EML and PIN OSA package are key technique, through I2C system can contact with module.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Storage Temperature	Tst	-20	85	℃
Case Operating Temperature	Top	0	70	℃
Humidity(non-condensing)	Rh	5	95	%
Damage threshold, each lane	THd	6.3		dBm

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case temperature	Tca	0		70	℃
Signal Rate per Electrical Channel (8 x 25Gor26G)		-	25.78125 or 26.5625	-	Gbps
Signal Rate per Optical Channel (4 x 53G)		-	53.125	-	Gbps
Humidity	Rh	5		85	%
Power Dissipation	Pm			9	W

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter					
Differential voltage pk-pk	Vin, pp			900	mV
Common mode noise	RMS			17.5	mV
Differential termination resistance mismatch				10	%
Transition time	Trise/Tfall	10			ps
Common mode voltage	Vcm	-0.3		2.8	V
Eye width at 10-15 probability	EW15	0.46			UI
Eye height at at 10-15 probability	Limit 1	95			mV
	Limit 2	80			mV
Receiver					
Differential voltage pk-pk	Vout, pp			900	mV
Common mode voltage	Vcm	-0.35		2.8	V
Common mode noise	RMS			17.5	mV
Transition time	Trise/Tfall	9.5			ps
Vertical eye closure	VEC			5.5	dB
Eye width at 10-15 probability	EW15	0.57			UI
Eye height at at 10-15 probability	EH15	228			mV

Note：

1. Differential input voltage amplitude is measured between TxnP and TxnN.
2. Differential output voltage amplitude is measured between RxnP and RxnN.

Optical Characteristics

Table 3 - Optical Characteristics

Parameters	Min	Type	Max	Unit	Notes
Transmitter					
Signaling speed per lane	26.5625 ± 100 ppm			GBd	
Transmit wavelengths	1294.53		1296.59	nm	
	1299.02		1301.09		
	1303.54		1305.63		
	1308.09		1310.19		
Total average launch power			11.3	dBm	
Average launch power, each lane	-3.4		5.3	dBm	
Optical modulation amplitude (OMA), each lane	-0.4		5.1	dBm	
Extinction ratio (ER)	3.5			dB	
Side-mode suppression ratio (SMSR)	30			dB	
Launch power in OMA minus TDECQ, each lane For ER>4.5dB For ER<4.5dB	 -1.8 -1.7			dBm	
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane			3.2	dB	
Average launch power of OFF transmitter, each lane (max)			-30	dBm	

Parameters	Min	Type	Max	Unit	Notes
$^{RIN}15.6^{OMA}$			-132	dB/Hz	
Optical return loss tolerance			15.6	dB	
Transmitter reflectance			-26	dB	
Receiver					
Signaling speed per lane	26.5625 ± 100 ppm			GBd	
Receive wavelengths	1294.53		1296.59	nm	
	1299.02		1301.09		
	1303.54		1305.63		
	1308.09		1310.19		
Average receiver power, each lane	-9.7		5.3	dBm	
Receiver power, each lane (OMA)			5.1	dBm	
Difference in receive power between any two lanes (OMA)			4.2	dB	
Damage threshold, each lane	6.3			dBm	
Receiver sensitivity (OMA), each lane			RS	dBm	1
LOS assert	-25.7			dBm	
LOS deassert			-11.7	dBm	
LOS hysteresis	0.5			dB	
Receiver reflectance			-26	dB	

Note：

1. RS=max (-7.2, SECQ -8.6) dBm, BER@2E 4, Pre-FEC

Pin Description

Table 1- Pad Function Definition

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power mode;	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note 1: QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 7. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

Note 3: All Vendor Specific, Reserved, No Connect and ePPS (if not used) pins may be terminated with 50 Ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A,1B will then occur simultaneously, followed by 2A,2B,followed by 3A,3B.

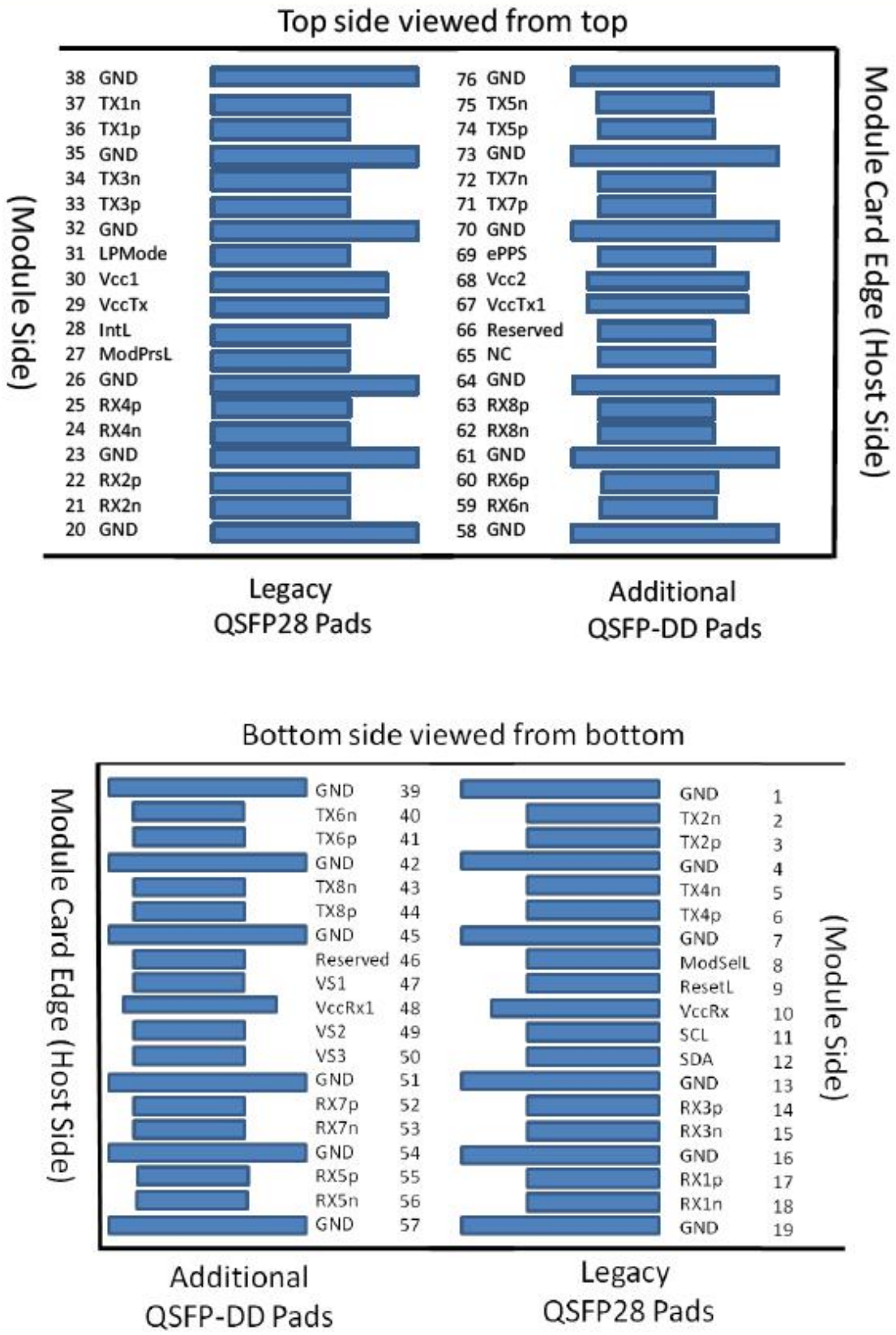


Figure2. Electrical Pin-out Details

ModSelL Pin

The ModSelL is an input signal that shall be pulled to Vcc in the QSFP-DD module. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When ModSelL is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host.
In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP-DD modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL Pin

The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state.

LPMode Pin

LPMode is an input signal. The LPMode signal shall be pulled up to Vcc in the QSFP-DD module. LPMode is used in the control of the module power mode. See CMIS Section 6.3.1.3.

ModPrsL Pin

ModPrsL shall be pulled up to Vcc Host on the host board and pulled low in the module. The ModPrsL is asserted “Low” when the module is inserted. The ModPrsL is deasserted “High” when the module is physically absent from the host connector due to the pull-up resistor on the host board.

IntL Pin

IntL is an output signal. The IntL signal is an open collector output and shall be pulled to Vcc Host on the host board. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is deasserted “High” after all set interrupt flags are read.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure3.

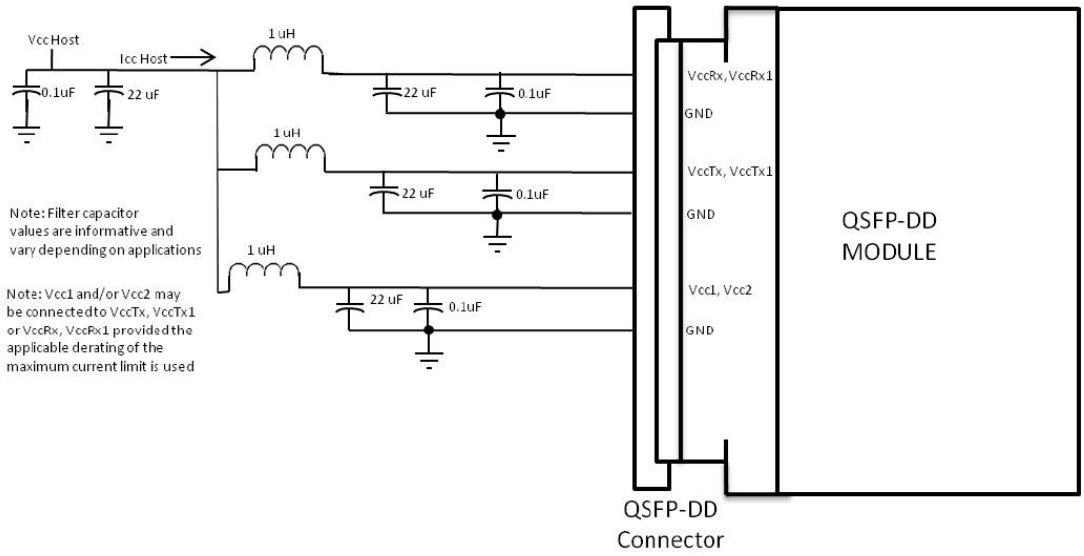


Figure3. Host Board Power Supply Filtering

Optical Interface Lanes and Assignment

The optical interface port is Duplex LC connector.

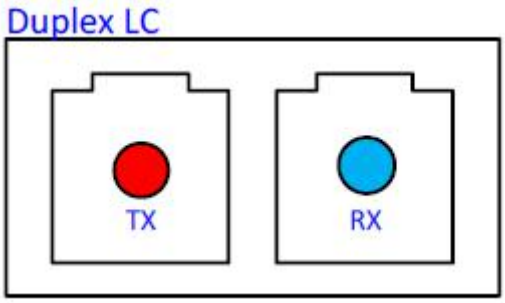


Figure 4. Optical Receptacle

DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics monitoring function is available on all Gigalight QSFP DD products. A 2-wire serial interface provides user to contact with module.

Memory Structure and Mapping

This limits the management memory that can be directly accessed by the host to 256 bytes, which is divided in Lower Memory (addresses 00h through 7Fh) and Upper Memory (addresses 80h through FFh).

A larger addressable management memory is required for all but the most basic modules. This is supported by a structure of 128-byte pages, together with a mechanism for dynamically mapping any of the 128-byte pages from a larger internal management memory space into Upper Memory the host addressable space.

The addressing structure of the additional internal management memory is shown in Figure 5. The management memory inside the module is arranged as a unique and always host accessible address space of 128 bytes (Lower Memory) and as multiple upper address subspaces of 128 bytes each (Pages), only one of which is selected as host visible in Upper Memory. A second level of Page selection is possible for Pages for which several instances exist (e.g. where a bank of pages with the same Page number exists).

This structure supports a flat 256 byte memory for passive copper modules and permits timely access to addresses in the Lower Memory, e.g. Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function in the Lower Page. For more complex modules which require a larger amount of management memory the host needs to use dynamic mapping of the various Pages into the host addressable Upper Memory address space, whenever needed.

Note: The management memory map has been designed largely after the QSFP memory map. This memory map has been changed in order to accommodate 8 electrical lanes and to limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

Supported Pages

A basic 256 byte subset of the Management Memory Map is mandatory for all CMIS compliant devices. Other parts are only available for paged memory modules, or when advertised by the module. See CMIS V4.0 for details regarding the advertisement of supported management memory spaces.

In particular, support of the Lower Memory and of Page 00h is required for all modules, including passive copper cables. These pages are therefore always implemented. Additional support for Pages 01h, 02h and bank 0 of Pages 10h and 11h is required for all paged memory modules.

Bank 0 of pages 10h-1Fh, provides lane-specific registers for the first 8 lanes, and each additional bank provides support for additional 8 lanes. Note, however, that the allocation of information over the banks may be page specific and may not to be related to grouping data for 8 lanes.

The structure allows address space expansion for certain types of modules by allocating additional Pages. Moreover, additional banks of pages

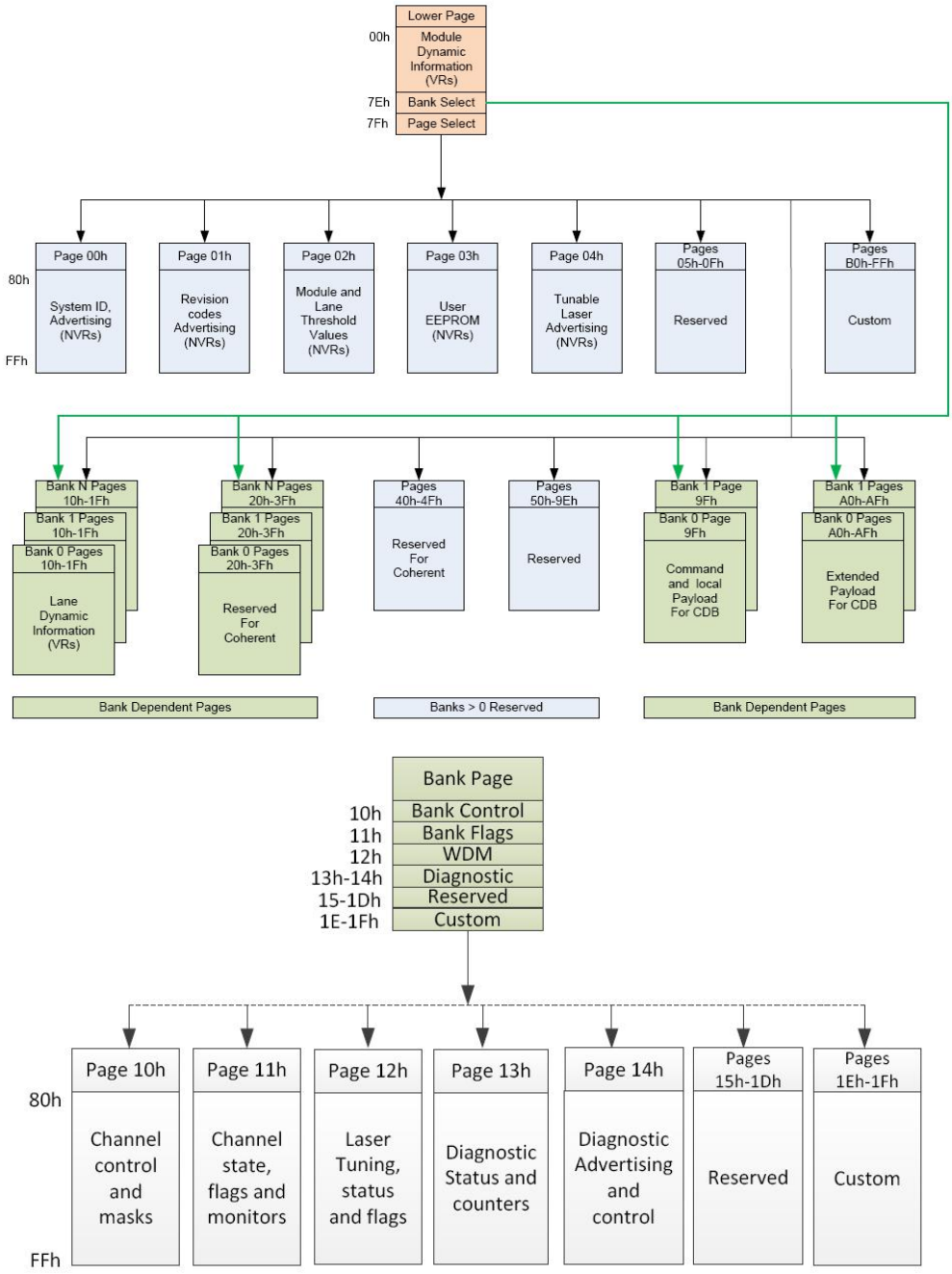


Figure5. QSFP DD Memory Map

Mechanical Dimensions

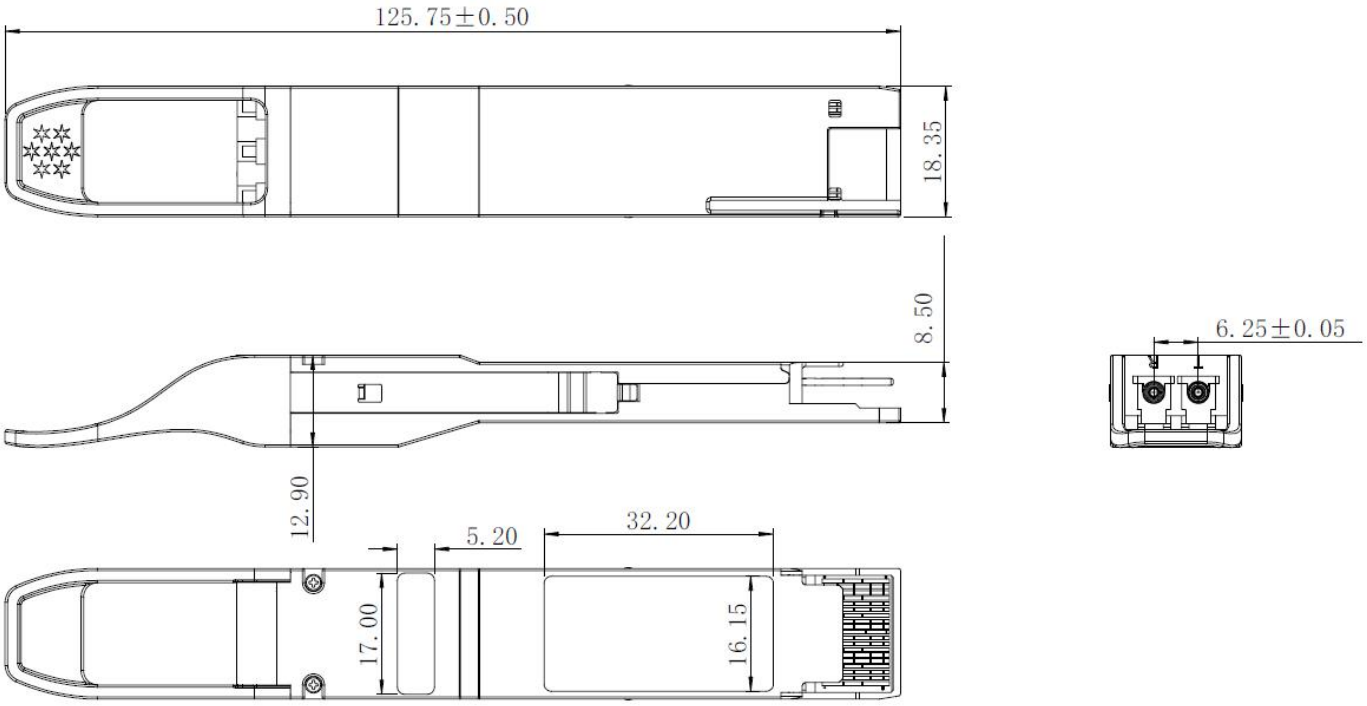


Figure6. Mechanical Specifications

Regulatory Compliance

Gigalight GQD-SPO201-LR4CZ transceivers are Class 1 Laser Products. They are certified per the following standards:

Feature	Standard
Laser Safety	IEC 60825-1:2014 (3rd Edition) IEC 60825-2:2004/AMD2:2010 EN 60825-1-2014 EN 60825-2:2004+A1+A2
Electrical Safety	EN 62368-1: 2014 IEC 62368-1:2014 UL 62368-1:2014
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863
CE EMC	EN55032：2015 EN55035：2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B; ANSI C63.4-2014

References

1. QSFP DD MAS Rev5.0

2. CMIS V4.0
3. IEEE802.3cn 200GBASE-LR4
4. OIF CEI-28G-VSR

⚠CAUTION:
Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering information

Part Number	Product Description
GQD-SPO201-LR4CZ	QSFP DD, 200G, 10km on SMF(LWDM), with DSP Power consumption <9W, duplex LC connector.

Important Notice

Performance figures, data and any illustrative material provided in this data sheet are typical and must be specifically confirmed in writing by GIGALIGHT before they become applicable to any particular order or contract. In accordance with the GIGALIGHT policy of continuous improvement specifications may change without notice.

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Revision History

Revision	Date	Description
V0	May-16-2023	Advance Release.