GIGALIGHT 200G QSFPDD LR8 Optical Transceiver Module

P/N: GQD-SPO201-LR8C

Features

- 8 channels full-duplex transceiver modules
- Transmission data rate up to 26Gbps per channel
- 8 x 26Gb/s DFB-based LAN-WDM Cooling transmitter
- 8 channels PIN ROSA
- Internal CDR circuits on both receiver and transmitter channels
- Support CDR bypass
- Low power consumption <7.5W
- Hot Pluggable QSFP DD form factor and Compliant with CMIS
- Up to 10km reach for G.652 SMF
- Duplex LC receptacles
- Built-in digital diagnostic functions
- Operating case temperature 0℃ to +70℃
- 3.3V power supply voltage
- RoHS2.0 compliant (lead free)

Applications

- IEEE 802.3ba 100GBASE-LR4

Description

The Gigalight Technologies GQD-SPO201-LR8C is an Eight-Channel, Pluggable, Fiber-Optic QSFP DD LR8 for 2×100 Gigabit Ethernet Applications. This transceiver is a high performance module for data communication and interconnect applications. It integrates eight data lanes in each direction with 208Gbps bandwidth. Each lane can operate at 26Gbps up to 10km over G.652 SMF. These modules are designed to operate over singlemode fiber systems using LAN-WDM 8 wavelengths. The electrical interface uses a 76 contact edge type connector. The optical interface uses duplex LC connector. This module incorporates Gigalight Technologies proven circuit and Optical technology to provide reliable long life, high performance, and consistent service.

200G QSFP DD LR8 CIRCUIT STRUCTURE

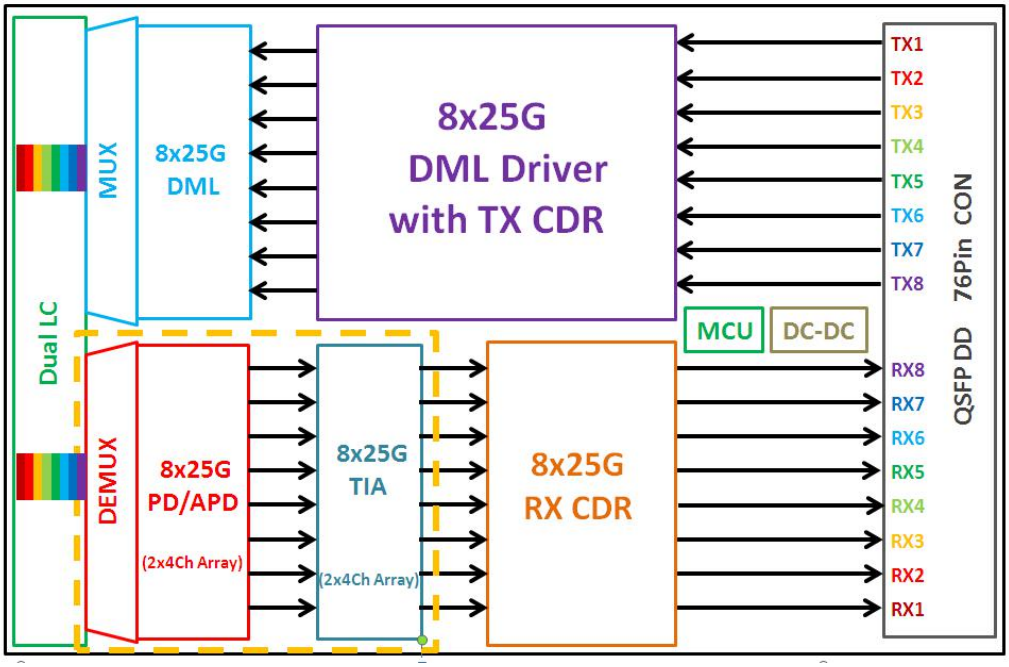


Figure1. Module Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-20	85	℃
Case Operating Temperature	Top	0	70	℃
Humidity(non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	V_{cc}	3.13	3.3	3.47	V
OperatingCase Temperature	T_c	0		70	℃
Data Rate Per Lane	fd		25.78125		Gbps
Humidity	Rh	5		85	%
Power Dissipation	P_m			7.5	W
Fiber Bend Radius	R_b	0.002		10	km

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential Input Impedance	Z_{in}	90	100	110	ohm
Differential Output Impedance	Z_{out}	90	100	110	ohm
Differential Input Voltage Amplitude[1]	ΔV_{in}	190		700	mVp-p
Differential Output Voltage Amplitude[2]	ΔV_{out}	300		850	mVp-p
Input Logic Level High	V_{IH}	2.0		V_{cc}	V
Input Logic Level Low	V_{IL}	0		0.8	V
Output Logic Level High	V_{OH}	V_{cc}-0.5		V_{cc}	V
Output Logic Level Low	V_{OL}	0		0.4	V

Note:

1. Differential input voltage amplitude is measured between TxnP and TxnN.
2. Differential output voltage amplitude is measured between RxnP and RxnN.

Optical Characteristics

Table 3 - Optical Characteristics

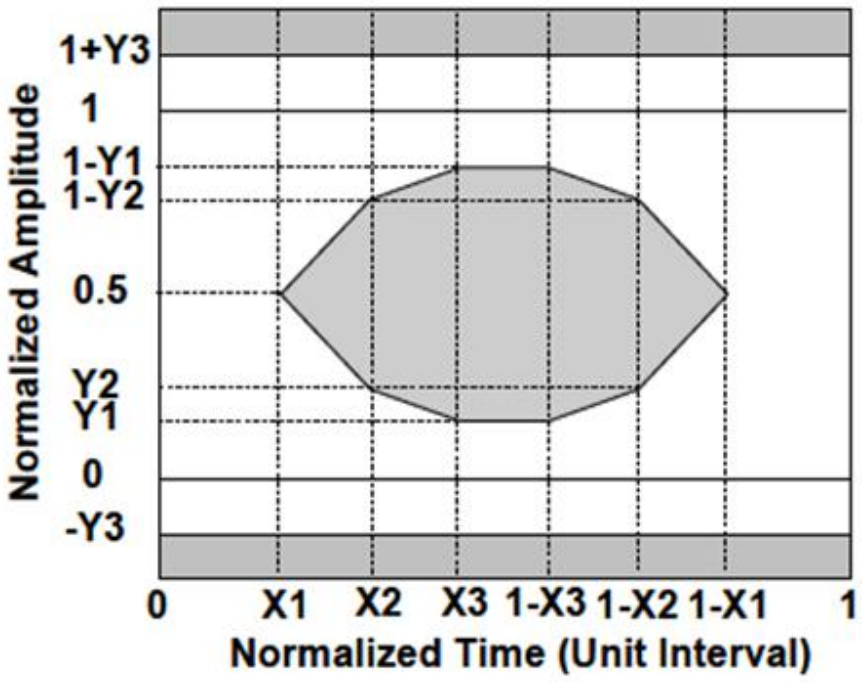
100GBASE-LR4						
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**	**Notes**
Lane Wavelength	L0	1272.55	1273.54	1274.54	nm	
	L1	1276.89	1277.89	1278.89	nm	
	L2	1281.25	1282.26	1283.27	nm	
	L3	1285.65	1286.66	1287.68	nm	
	L4	1294.53	1295.56	1296.59	nm	
	L5	1299.02	1300.05	1301.09	nm	
	L6	1303.54	1304.58	1305.63	nm	
	L7	1308.09	1309.14	1310.19	nm	
Transmitter						
SMSR	SMSR	30			dB	
Total Average Launch Power	P_T			10.5	dBm	
Average Launch Power, each Lane	P_{AVG}	-4.3		4.5	dBm	
OMA, each Lane	P_{OMA}	-1.3		4.5	dBm	1
Difference in Launch Power between any Two Lanes (OMA)	Ptx,diff			5	dB	
Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane		-2.3			dBm	
TDP, each Lane	TDP			2.2	dB	
Extinction Ratio	ER	4			dB	

100GBASE-LR4						
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**	**Notes**
$RIN_{20}OMA$	RIN			-130	dB/Hz	
Optical Return Loss Tolerance	TOL			20	dB	
Transmitter Reflectance	R_T			-12	dB	
Eye Mask coordinates: X1, X2, X3, Y1, Y2, Y3		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				2
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	
Receiver						
Damage Threshold, each Lane	TH_d	5.5			dBm	3
Total Average Receive Power				10.5	dBm	
Average Receive Power, each Lane		-10.6		4.5	dBm	
Receive Power (OMA), each Lane				4.5	dBm	
Receiver Sensitivity (OMA), each Lane	SEN			-8.6	dBm	
Stressed Receiver Sensitivity (OMA), each Lane				-6.8	dBm	4
Difference in Receive Power between any Two Lanes (OMA)	Prx,diff			5.5	dB	
LOS Assert	LOSA		-18		dBm	
LOS Deassert	LOSD		-15		dBm	
LOS Hysteresis	LOSH	0.5			dB	
Receiver Electrical 3 dB upper Cutoff Frequency,	Fc			31	GHz	

100GBASE-LR4						
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**	**Notes**
each Lane						
Conditions of Stress Receiver Sensitivity Test (Note 5)						
Vertical Eye Closure Penalty, each Lane			1.8		dB	5
Stressed Eye J2 Jitter, each Lane			0.3		UI	
Stressed Eye J9 Jitter, each Lane			0.47		UI	

Note:

1. Even if the TDP < 1 dB, the OMA min must exceed the minimum value specified here.
2. See Figure 4 below.
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
4. Measured with conformance test signal at receiver input for BER = $1x10^{-12}$.
5. Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.



Pin Description

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power mode;	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note 1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 7. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

Note 3: All Vendor Specific, Reserved, No Connect and ePPS (if not used) pins may be terminated with 50 Ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A,1B will then occur simultaneously, followed by 2A,2B,followed by 3A,3B.

.3

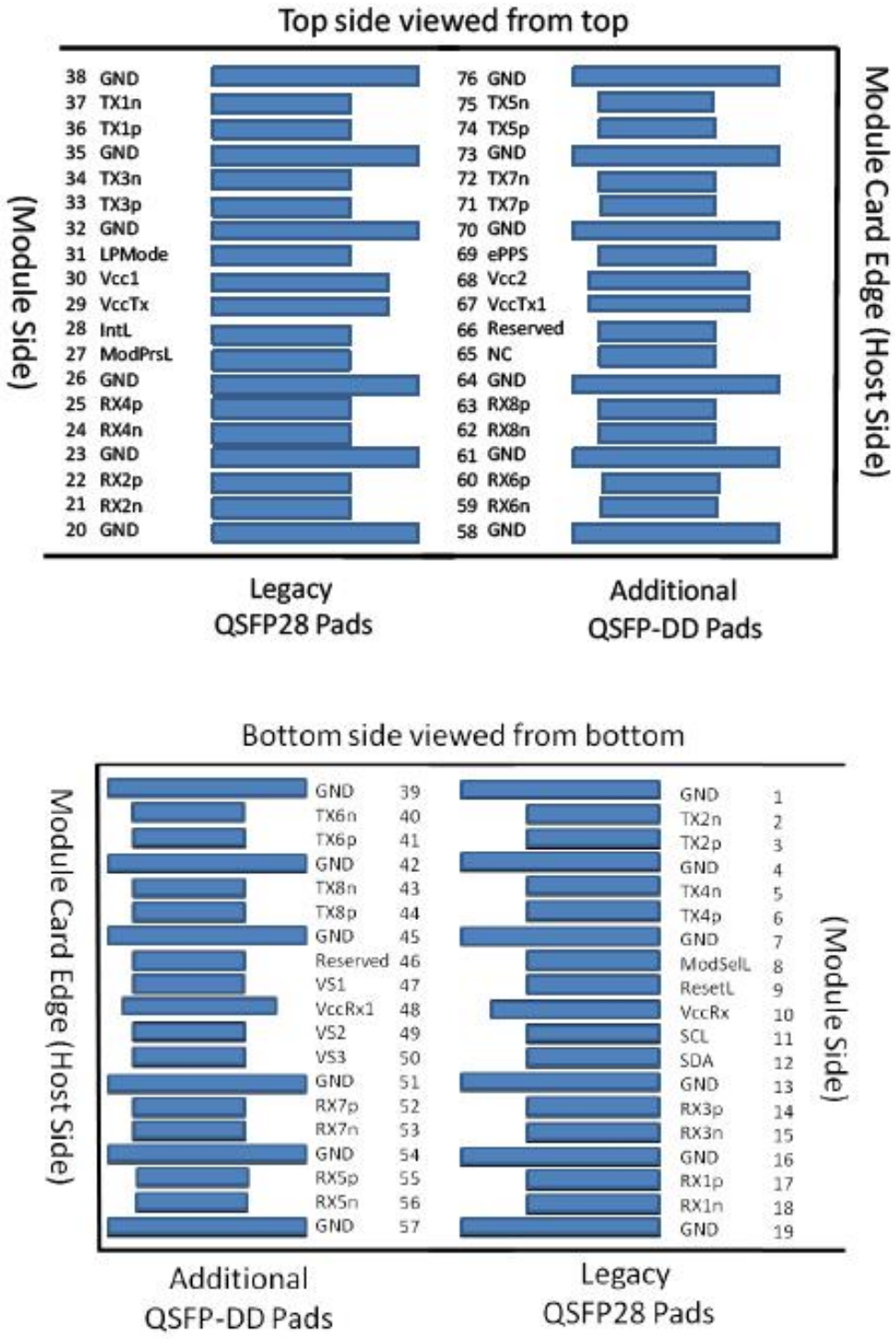


Figure2. Electrical Pin-out Details

ModSelL Pin

The ModSelL is an input signal that must be pulled to Vcc in the QSFP-DD module. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When ModSelL is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP-DD modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL Pin

The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) (See Table 13) initiates a complete module reset, returning all user module settings to their default state.

LPMode Pin

LPMode is an input signal. The LPMode signal shall be pulled up to Vcc in the QSFP-DD module (see Table 2). LPMode is used in the control of the module power mode.
See CMIS Section 6.3.1.3.

ModPrsL Pin

ModPrsL must be pulled up to Vcc Host on the host board and grounded in the module. The ModPrsL is asserted “Low” when the module is inserted and deasserted “High” when the module is physically absent from the host connector.

IntL Pin

IntL is an output signal. The IntL signal is an open collector output and must be pulled to Vcc Host on the host board. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host

identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is deasserted “High” after all set interrupt flags are read.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure3.

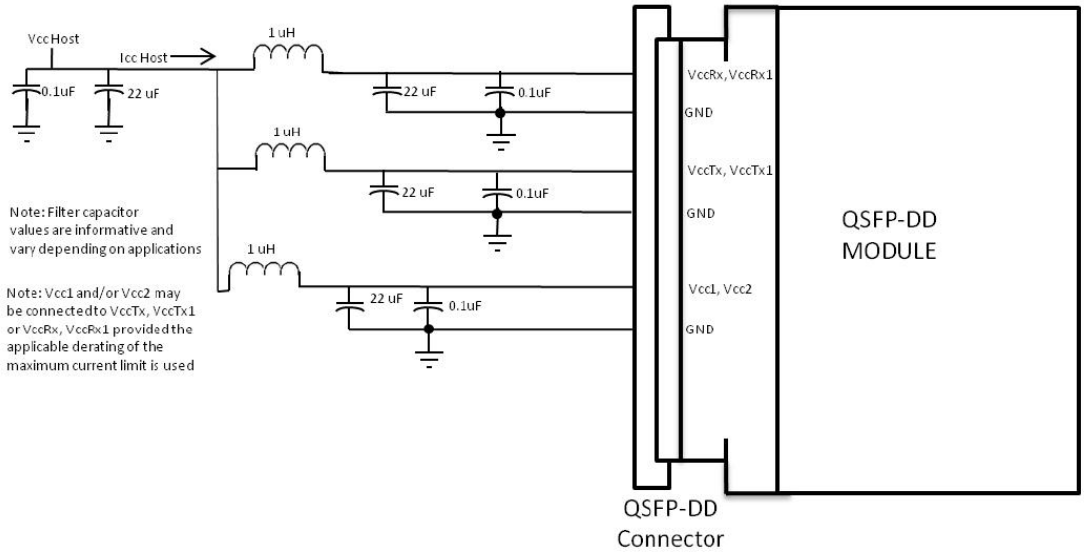


Figure3. Host Board Power Supply Filtering

DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics monitoring function is available on all Gigalight QSFP DD products. A 2-wire serial interfaceprovides user to contact with module.

This subsection defines the Memory Map for a CMIS Module used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all CMIS devices. The interface has been designed largely after the QSFP memory map. The memory map has been changed in order to accommodate 8 electrical lanes and limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

The structure of the memory is shown in Figure 5 . The memory space is arranged into a

lower, single page, address space of 128 bytes and multiple upper address space pages. This structure supports a flat 256 byte memory for passive copper cables and permits timely access to addresses in the lower page, e.g. Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function. The structure also provides address expansion by adding additional upper 1pages as needed. Upper pages 00-02 all contain static, non-volatile advertising registers. Upper page 01 provides revision codes and advertising registers that indicate the capabilities of the module. Upper page 02 provides thresholds for monitored functions. Upper page 03 provides a user read/write space. The lower page and upper page 00 are required for passive copper cables and are always implemented. In addition, upper pages 1, 2 and bank 0 pages 10h and 11h are required for active modules. See CMIS Document Table 40 for details regarding the implementation of optional upper pages and the bank pages.

Bank pages are provided to provide the ability to support modules with more than 8 lanes. Bank 0 provides lane-specific registers for the lower 8 lanes. Each additional bank provides support for an additional 8 lanes.

Reserved bytes are for future use and shall not be used and shall be set to 0. Other organizations shall contact the managing organization or the editor of this document to request allocations of registers. The use of custom bytes is not restricted and may be vendor defined. The use of registers defined as custom may be subject to additional agreements between module users and vendors.

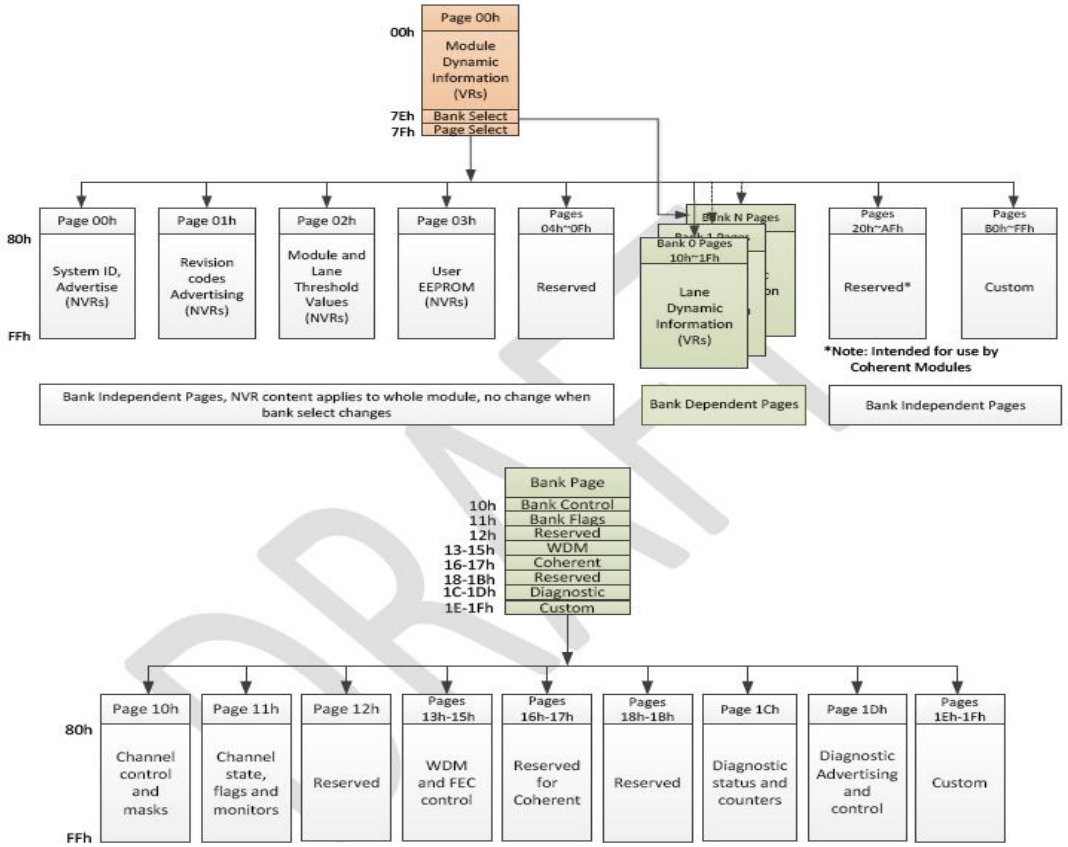


Figure4. QSFP DD Memory Map

Mechanical Dimensions

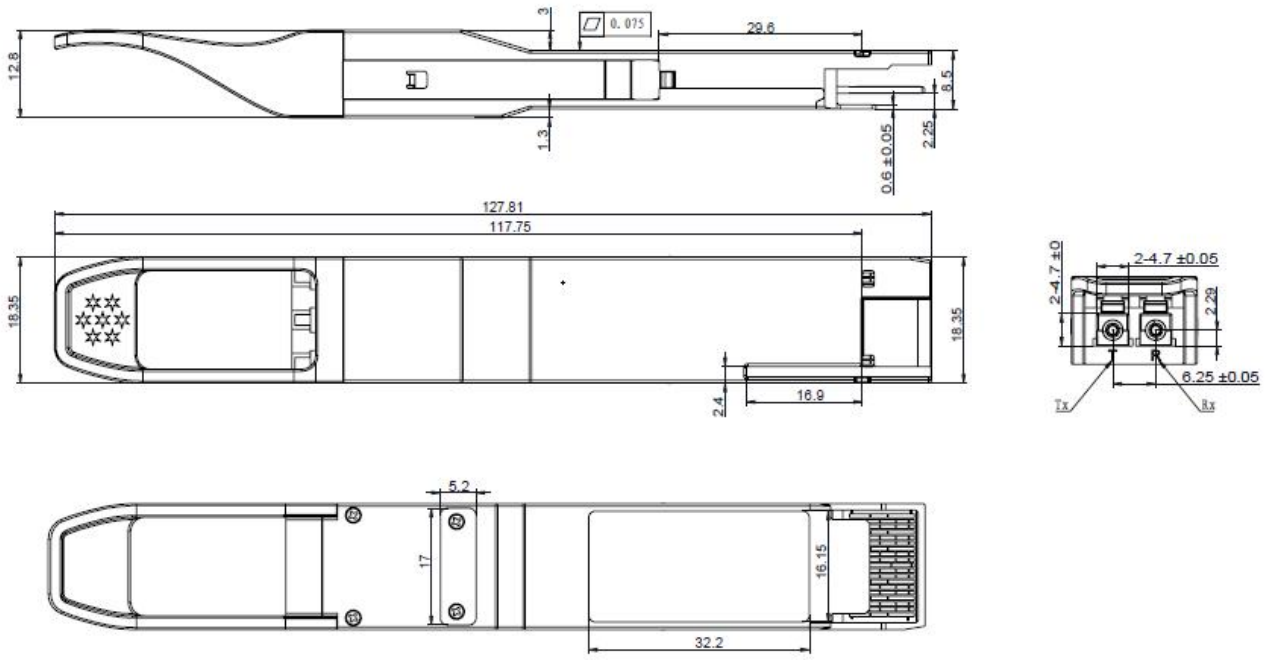


Figure5. Mechanical Specifications

Regulatory Compliance

Gigalight GQD-SPO201-LR8C transceivers are Class 1 Laser Products. They are compliant with the following standards:

Feature	Standard
Laser Safety	IEC 60825-1:2014 (3rd Edition) IEC 60825-2:2004/AMD2:2010 EN 60825-1-2014 EN 60825-2:2004+A1+A2
Electrical Safety	EN 62368-1: 2014 IEC 62368-1:2014 UL 62368-1:2014
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863
CE EMC	EN55032：2015 EN55035：2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B ANSI C63.4-2014

References

1. QSFP DD MAS Rev5.0
2. CMIS V4.0
3. IEEE802.3ba 100GBASE-LR4
4. OIF CEI-528G-VSR

⚠CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering information

Part Number	Product Description
GQD-SPO201-LR8C	QSFP DD, 2x100GBASE-LR4, Duplex LC,up to 10km G.652 SMF

Important Notice

Performance figures, data and any illustrative material provided in this data sheet are typical and must be specifically confirmed in writing by GIGALIGHT before they become applicable to any particular order or contract. In accordance with the GIGALIGHT policy of continuous improvement specifications may change without notice.

The publication of information in this data sheet does not imply freedom from patent or other protective rights of GIGALIGHT or others. Further details are available from any GIGALIGHT sales representative.

E-mail: sales@gigalight.com
Official Site: www.gigalight.com

Revision History

Revision	Date	Description
V0	Sep 14, 2020	Advance Release.
V1	Apr-17-2021	Modify Regulatory Compliance.