


SFP28 1310nm 32G FC 25km Transceiver

GSS-SPO280-L2C

Features

- ✓ Hot-pluggable SFP28 form factor
- ✓ Supports 28.05Gbps aggregate bit rate
- ✓ Maximum link length of 25km over SMF
- ✓ 1310nm DFB laser and APD photo-detector
- ✓ Internal CDR on both Transmitter and Receiver channel
- ✓ Duplex LC receptacle
- ✓ Single 3.3V power supply
- ✓ Power dissipation < 1.8W
- ✓ RoHS compliant and lead free) 
- ✓ Industrial case temperature range: 0°C to 70°C



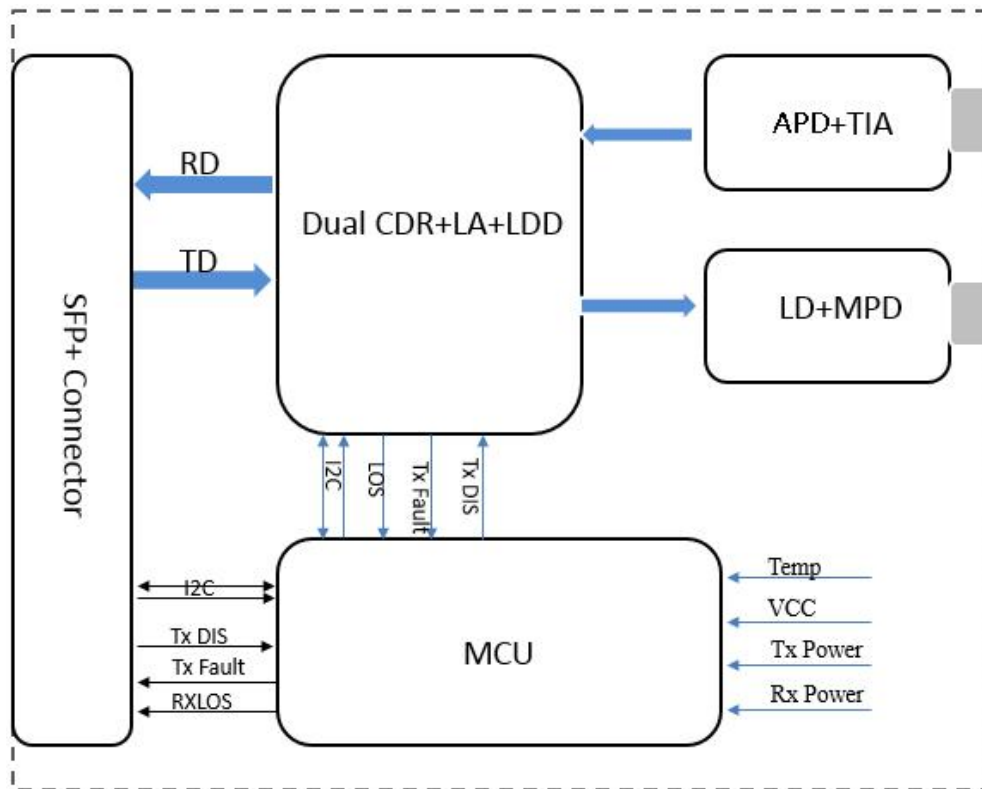
Applications

- ✓ CPRI Option 10
- ✓ 25G Ethernet
- ✓ 32G FC

Description

This product is a 32G FC SFP28 transceiver designed for optical communication compliant with 25GE and 32G FC standard. It is DFB transmitter and high sensitivity APD receiver provide superior performance for 25GE and 32G FC application up to 25km (with FEC) Links. This module is designed to operate over single mode fiber systems using a nominal wavelength of 1310nm. The optical interface uses duplex LC receptacle. This module incorporates Gigalight Technologies proven circuit and technology to provide reliable long life, high performance, and consistent service. Compliance with IEEE802.3cc & SFF-8472.

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	Vcc	0	3.6	V
Storage Temperature	Ts	-40	+85	°C
Operating Humidity	-	0	85	%

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Case Temperature	Tc	0		+70	°C
Power Supply Voltage	Vcc	3.13	3.3	3.47	V
Power Supply Current	Icc			545	mA

Electrical Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Differential	Zin	90	100	110	ohm
Differential	Zout	90	100	110	ohm
Differential	ΔV_{in}	300		1100	mVp-p
Differential	ΔV_{out}	300		800	mVp-p
Input Logic	V _{IH}	2.0		V _{cc}	V
Input Logic	V _{IL}	0		0.8	V
Output Logic	V _{OH}	V _{cc} -0.5		V _{cc}	V
Output Logic	V _{OL}	0		0.4	V

Notes:

1. Differential input voltage amplitude is measured between TxnP and TxnN.
2. Differential output voltage amplitude is measured between RxnP and RxnN.

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Data rate	BR		28.05	-	Gbps	
Centre Wavelength	λ_c	1295		1325	nm	
Spectral Width (-20dB)	σ			1	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power	P _{out}	-5		3	dBm	
Optical Modulation Aptitude	OMA	-2			dBm	
Extinction Ratio	ER	3			dB	
Eye Mask Coordinates		{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}				
Receiver						
Data rate	BR		28.05		Gbps	
Centre Wavelength	λ_c	1295		1325	nm	
Average Power at Receiver		-20		-5	dBm	
Receive Reflectance(max)				-26	dB	
Receiver Sensitivity in OMA ¹	RS _{oma}	-	-	-15.5	dBm	
LOS De-Assert	LOS _D			-20	dBm	
LOS Assert	LOS _A	-33			dBm	
LOS Hysteresis		0.5			dB	

Note:

1. Hit Ratio =5×10⁻⁵. Unstressed receiver OMA sensitivity.

Timing and Electrical

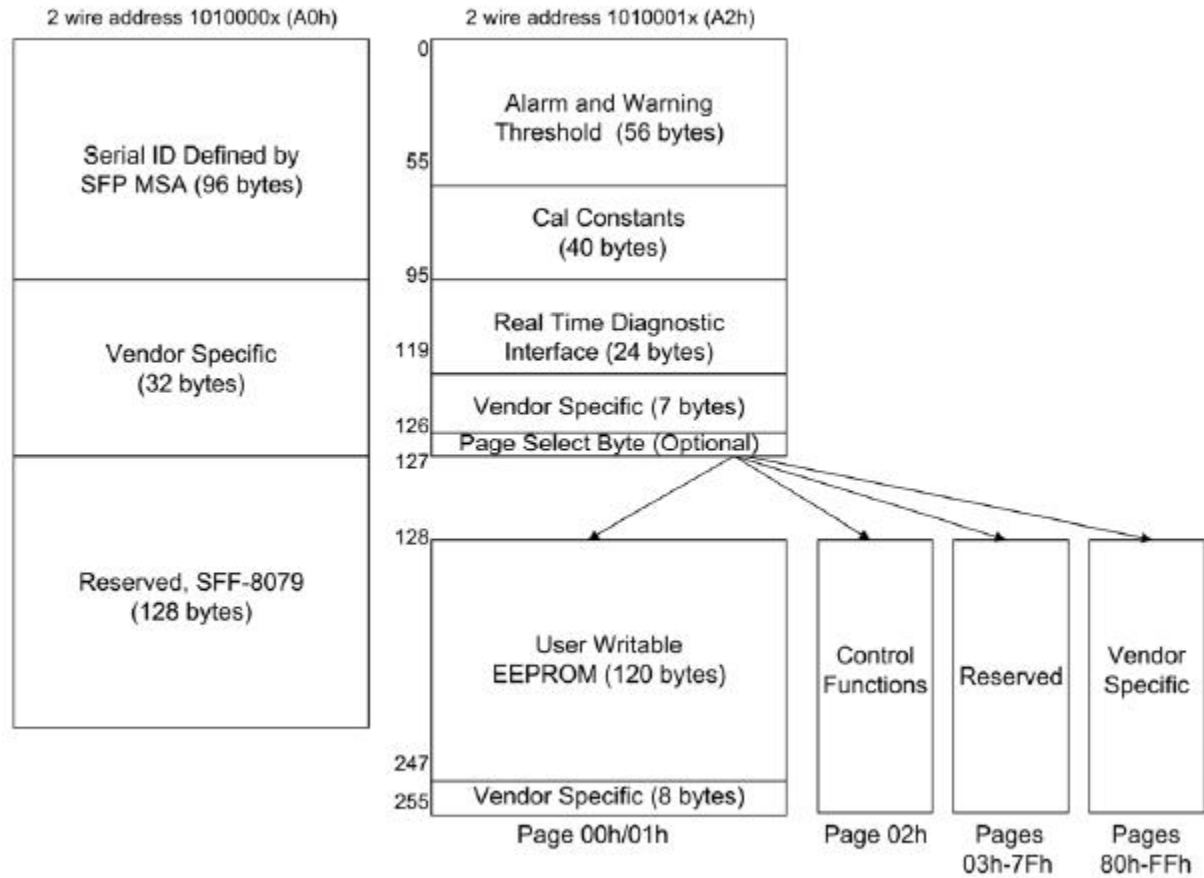
Parameter	Symbol	Min	Max	Unit	Conditions
Tx_Disable assert time	t_off		100	us	Rising edge of Tx_Disable to fall of output signal below 10% of nominal
Tx_Disable negate time	t_on		2	ms	Falling edge of Tx_Disable to rise of output signal above 90% of nominal. This only applies in normal operation, not during start up or fault recovery.
Time to initialize 2-wire interface	t_2w_start_up		300	ms	From power on or hot plug.
Time to initialize	t_start_up		300	ms	From power on or hot plug or Tx disable negated during power up.
					or Tx_Fault recovery, until non-cooled power level I part (or non-cooled power level II part already enabled at power level II for Tx_Fault recovery) is fully operational.
Time to initialize cooled module and time to power up a cooled module to Power Level II	t_start_up_cooled		90	s	From power on or hot plug, or Tx disable negated during power up or Tx_Fault recovery, until cooled power level I part (or cooled power level II part during fault recovery) is fully operational. Also, from stop bit low-to-high SDA transition enabling Power Level II until cooled module is fully operational
Time to Power Up to Level II	t_power_level2		300	ms	From stop bit low-to-high SDA transition enabling power level II until non-cooled module is fully operational
Time to Power Down from Level II	t_power_down		300	ms	From stop bit low-to-high SDA transition disabling power level II until module is within power level I requirements
Tx_Fault assert	Tx_Fault_on		1	ms	From occurrence of fault to assertion of Tx_Fault
Tx_Fault assert for cooled module	Tx_Fault_on_cooled		50	ms	From occurrence of fault to assertion of Tx_Fault
Tx_Fault Reset	t_reset	10		us	Time Tx_Disable must be held high to reset Tx_Fault
RS0, RS1 rate select timing for FC	t_RS0_FC, t_RS1_FC		500	us	From assertion till stable output
RS0, RS1 rate select timing non FC	t_RS0, t_RS1		24	ms	From assertion till stable output
Rx_LOS assert delay	t_los_on		100	us	From occurrence of loss of signal to assertion of Rx_LOS
Rx_LOS negate delay	t_los_off		100	us	From occurrence of presence of signal to negation of Rx_LOS

Memory Organization

The transceivers provide serial ID memory contents and diagnostic information about the present operating conditions by the 2-wire serial interface (SCL, SDA).

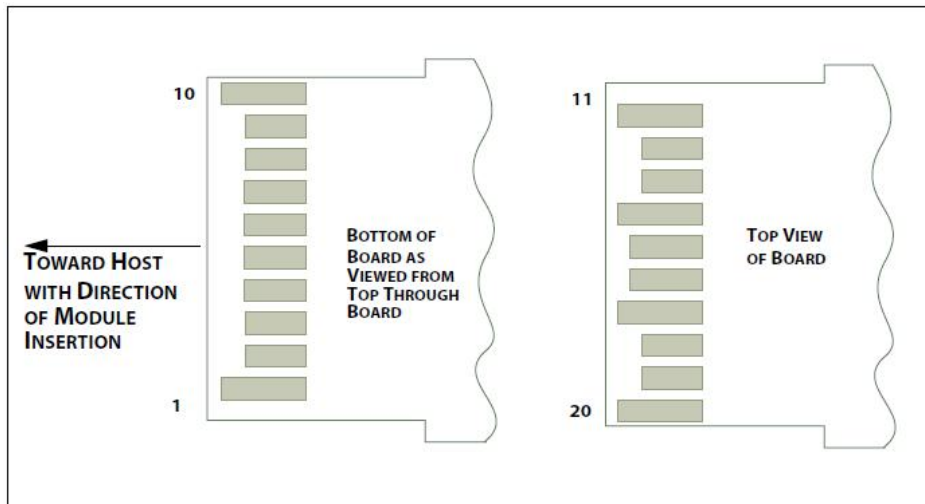
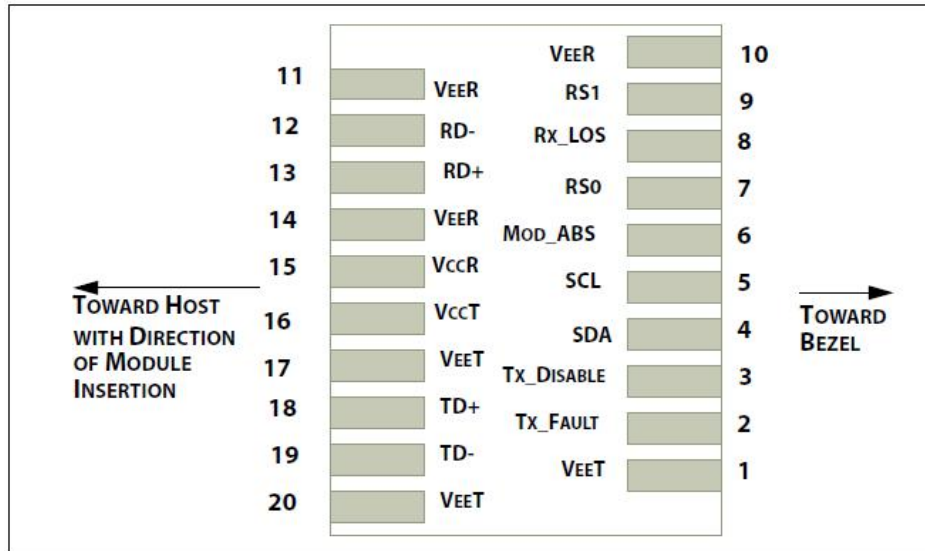
The memory map specific data field defines as following.

Two-wire Interface Fields



TWO-WIRE INTERFACE FIELDS

Pin Definitions



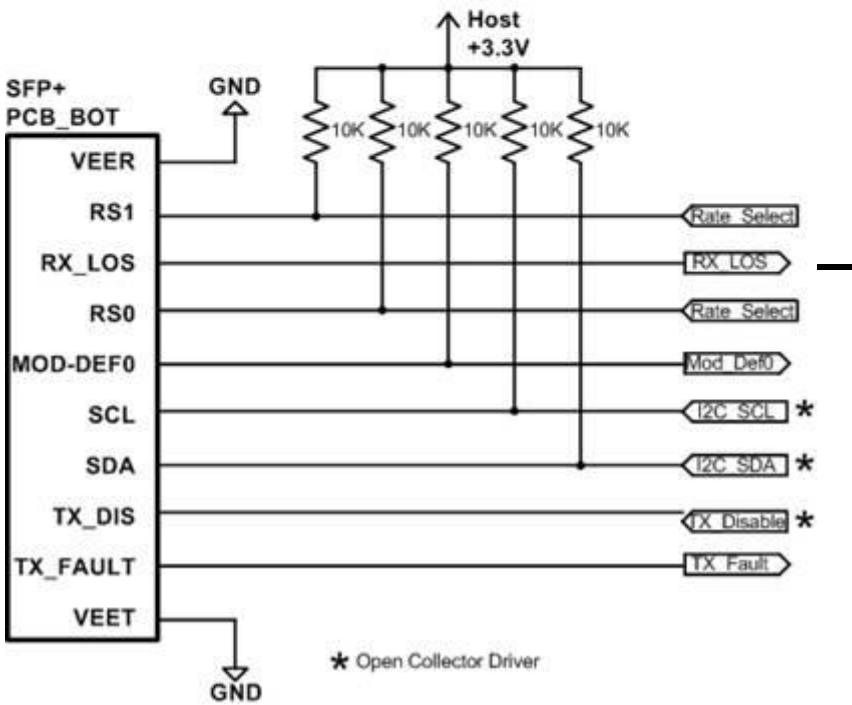
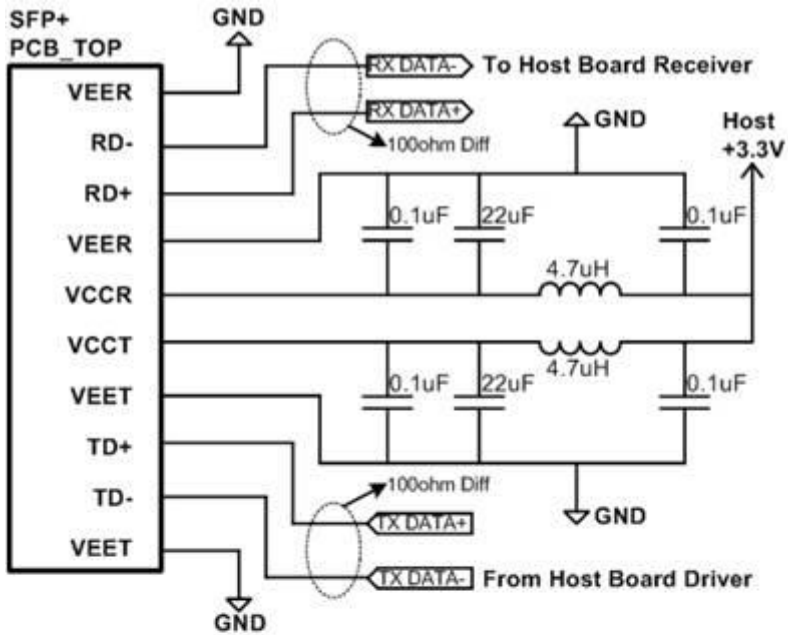
Pin Descriptions

PIN	Logic	Symbol	Name / Description	Note
1		VeeT	Module Transmitter Ground	1
2	LVTTL-O	TX_Fault	Module Transmitter Fault	2
3	LVTTL-I	TX_Dis	Transmitter Disable; Turns off transmitter laser output	
4	LVTTL-I/O	SDA	2-Wire Serial Interface Data Line	2
5	LVTTL-I	SCL	2-Wire Serial Interface Clock	2
6		MOD_ABS	Module Definition, Grounded in the module	
7	LVTTL-I	RS0	Receiver Rate Select	
8	LVTTL-O	RX_LOS	Receiver Loss of Signal Indication Active LOW	
9	LVTTL-I	RS1	Transmitter Rate Select (not used)	
10		VeeR	Module Receiver Ground	1
11		VeeR	Module Receiver Ground	1
12	CML-O	RD-	Receiver Inverted Data Output	
13	CML-O	RD+	Receiver Data Output	
14		VeeR	Module Receiver Ground	1
15		VccR	Module Receiver 3.3 V Supply	
16		VccT	Module Receiver 3.3 V Supply	
17		VeeT	Module Transmitter Ground	1
18	CML-I	TD+	Transmitter Non-Inverted Data Input	
19	CML-I	TD-	Transmitter Inverted Data Input	
20		VeeT	Module Transmitter Ground	1

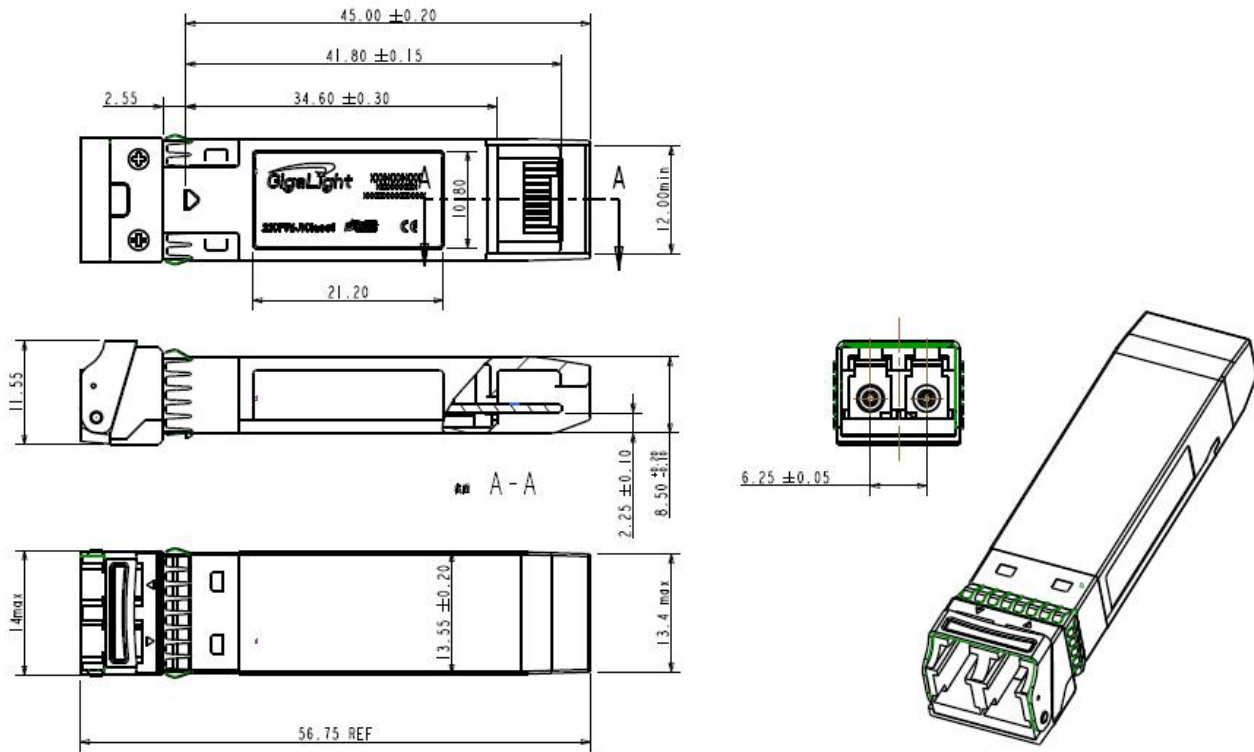
Notes:

1. Module ground pins GND are isolated from the module case.
2. Shall be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.45V on the host board.

Recommended Interface Circuit



Mechanical Dimensions



Regulatory Compliance

Gigalight GSS-SPO280-L2C transceivers are Class 1 Laser Products. They meet the requirements of the following standards.

Feature	Standard
Laser Safety	IEC 60825-1:2014 (3 rd Edition) IEC 60825-2:2021 EN 60825-1:2014+A11:2021 EN 60825-2:2004+A1+A2
Electrical Safety	EN 62368-1:2014/AC:2017 IEC 62368-1:2014 UL 62368-1:2014
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863
CE EMC	EN55032: 2015 EN55035: 2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B ANSI C63.4-2014

References

1. SFP28 MSA
2. Ethernet IEEE802.3cc
3. Directive 2011/65/EU of the European Parliament and of the Council, “on the restriction of the use of certain hazardous substances in electrical and electronic equipment,” July 1, 2011.

CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering information

Part Number	Product Description
GSS-SPO280-L2C	28.05Gbps, 1310nm; SFP28, 25km, 0°C ~ +70°C

Important Notice

Performance figures,data and any illustrative material provided in this data sheet are typical and must be



specifically confirmed in writing by Gigalight before they become applicable to any particular order or contract. In accordance with the Gigalight policy of continuous improvement specifications may change without notice.

The publication of information in this data sheet does not imply freedom from patent or other protective rights of Gigalight or others. Further details are available from any Gigalight sales representative.

Email: sales@gigalight.com.cn

<http://www.gigalight.com.cn>

Revision History

Revision	Date	Description
V0	Jun -15-2023	Advance Release.