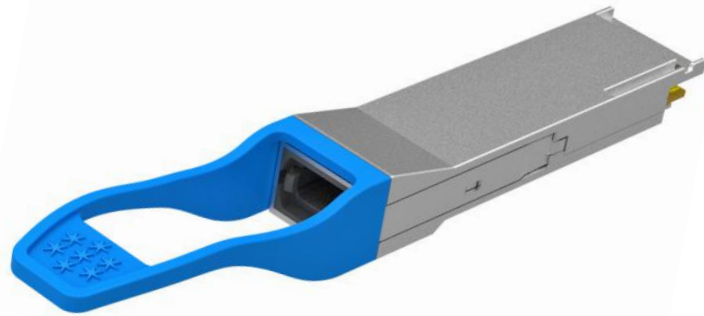


100Gbps QSFP28 PSM4 C-band DWDM Optical Transceiver Module P/N: GQS-Dxx101-124C

Features

- ✓ 4 channels full-duplex transceiver modules
- ✓ Transmission data rate up to 26Gbps per channel
- ✓ 4 channels C-band EML DWDM
- ✓ Compliant to ITU-T 694.1
- ✓ 4 channels PIN photo detector array
- ✓ Internal CDR circuits on both receiver and transmitter channels
- ✓ Support CDR bypass
- ✓ Low power consumption <5W
- ✓ Hot Pluggable QSFP form factor
- ✓ Up to 120km reach for G.652 SMF with external Mux/Demux,EDFA ,CD compensation
- ✓ Up to 10km reach for G.652 SMF without external CD compensation
- ✓ Single male MPO(APC 8-degree) connector receptacle
- ✓ Operating case temperature 0°C to +70°C
- ✓ 3.3V power supply voltage
- ✓ RoHS compliant(lead free)



Applications

- ✓ 100G Ethernet Metro-Access over DWDM
- ✓ P to P Access Network

Description

The Gigalight Technologies GQS-Dxx101-124C is a Four-Channel, Pluggable, Parallel, Fiber-Optic QSFP28 PSM4 for 100G or 40 Ethernet Metro-Access over DWDM applications. The transceiver is a high performance module for data communication and interconnect applications. It integrates four data lanes in each direction with 104 Gbps bandwidth. Each lane can operate at 26Gbps up to 120km over G.652 SMFwith external Mux/Demux,EDFA,CD compensation.The electrical interface uses a 38 contact edge type connector. The optical interface uses a 12 fiber MTP (MPO) connector. This module

incorporates Gigalight Technologies proven circuit and Optical technology to provide reliable long life, high performance, and consistent service.

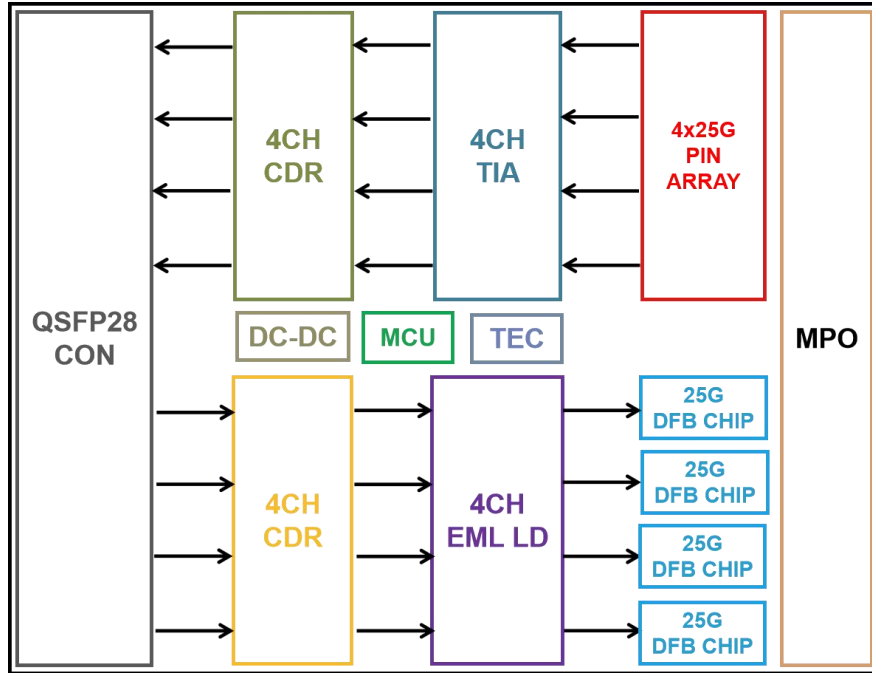


Figure1. Module Block Diagram

100Gb/s QSFP28 PSM4 C-band DWDM is one kind of parallel transceiver. DFB and PIN array package is key technique, through I2C system can contact with module.

Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-20	85	°C
Case Operating Temperature	Top	0	70	°C
Humidity(non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Supply Voltage	Vcc	3.13	3.3	3.47	V	

Operating Case temperature	Tca	0		70	°C	
Data Rate Per Lane	fd		25.78125		Gbps	
Humidity	Rh	5		85	%	
Power Dissipation	Pm			5	W	
Link Distance with G.652	D			120	km	1

Note:

- 1.Requires a DWDM line system with amplification and dispersion management.

Electrical Specifications

Table 2. Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential input impedance	Zin	90	100	110	ohm
Differential Output impedance	Zout	90	100	110	ohm
Differential input voltage amplitude	ΔV_{in}	190		700	mVp-p
Differential output voltage amplitude	ΔV_{out}	300		850	mVp-p
Input Logic Level High	V _{IH}	2.0		VCC	V
Input Logic Level Low	V _{IL}	0		0.8	V
Output Logic Level High	V _{OH}	VCC-0.5		VCC	V
Output Logic Level Low	V _{OL}	0		0.4	V

Note:

1. Differential input voltage amplitude is measured between TxnP and TxnN.
2. Differential output voltage amplitude is measured between RxnP and RxnN.

Optical Characteristics

Table 3. Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Centre Wavelength	λ_c	per ITU-T 694.1			nm	-
Side Mode Suppression Ratio	SMSR	30	-		dB	-

Average launch power, each lane	PAVG	-4.3		4.5	dBm	-
Optical Modulation Amplitude(OMA),each lane	POMA	-1.3		4.5	dBm	1
Extinction Ratio	ER	6	-	-	dB	-
Relative Intensity Noise	RIN			-128	dB/Hz	
Optical Return Loss Tolerance	TOL			20	dB	
Transmitter Reflectance	RT			-20	dB	
Average launch power of OFF transmitter, each lane	POFF			-30	dBm	-
Eye Mask coordinates: X1, X2, X3, Y1, Y2, Y3	{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}					Hit Ratio = 5x10 ⁻⁵
Receiver						
Centre Wavelength	λ_c	1200		1600	nm	-
Damage Threshold, each lane	THd	5.5			dBm	2
Average Receive Power, each lane		-10.6		4.5	dBm	
Receive power, each lane (OMA)				4.5	dBm	
Receiver Reflectance	RR			-26	dBm	
Receiver Sensitivity (OMA), each lane	SEN			-8.6	dBm	3
LOS Assert	LOSA		-18		dBm	-
LOS De-Assert – OMA	LOSD		-15		dBm	-
LOS Hysteresis	LOSH	0.5			dB	-

Note:

1. Even if the TDP<1dB, the OMA min must exceed the minimum value specified here.
2. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
3. Sensitivity is specified at 1x10⁻¹² BER at 25.78125 Gb/s.

C-band λ_c Wavelength Grid

Table 4. Wavelength Table

Product Code	TX1		TX2		TX3		TX4	
	Ch. No.	Frequency	Ch. No.	Frequency	Ch. No.	Frequency	Ch. No.	Frequency
		(THz)		(THz)		(THz)		(THz)
GQS-D13101-124C	C13	191.3	C14	191.4	C15	191.5	C16	191.6
GQS-D17101-124C	C17	191.7	C18	191.8	C19	191.9	C20	192
GQS-D21101-124C	C21	192.1	C22	192.2	C23	192.3	C24	192.4
GQS-D25101-124C	C25	192.5	C26	192.6	C27	192.7	C28	192.8
GQS-D29101-124C	C29	192.9	C30	193	C31	193.1	C32	193.2
GQS-D33101-124C	C33	193.3	C34	193.4	C35	193.5	C36	193.6
GQS-D37101-124C	C37	193.7	C38	193.8	C37	193.7	C37	193.7
GQS-D41101-124C	C41	194.1	C42	194.2	C43	194.3	C44	194.4
GQS-D45101-124C	C45	194.5	C46	194.6	C47	194.7	C48	194.8
GQS-D49101-124C	C49	194.9	C50	195	C51	195.1	C52	195.2
GQS-D53101-124C	C53	195.3	C54	195.4	C55	195.5	C56	195.6
GQS-D57101-124C	C57	195.7	C58	195.8	C59	195.9	C60	196

Pin Descriptions

Table 5. Pin Descriptions

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Module Ground	1
2	CML-I	Tx2-	Transmitter inverted data input	
3	CML-I	Tx2+	Transmitter non-inverted data input	
4		GND	Module Ground	1
5	CML-I	Tx4-	Transmitter inverted data input	
6	CML-I	Tx4+	Transmitter non-inverted data input	
7		GND	Module Ground	1
8	LVTTL-I	MODSEIL	Module Select	2

9	LVTTL-I	ResetL	Module Reset	2
10		VCCR _x	+3.3v Receiver Power Supply	
11	LVC MOS-I	SCL	2-wire Serial interface clock	2
12	LVC MOS-I/O	SDA	2-wire Serial interface data	2
13		GND	Module Ground	1
14	CML-O	RX3+	Receiver non-inverted data output	
15	CML-O	RX3-	Receiver inverted data output	
16		GND	Module Ground	1
17	CML-O	RX1+	Receiver non-inverted data output	
18	CML-O	RX1-	Receiver inverted data output	
19		GND	Module Ground	1
20		GND	Module Ground	1
21	CML-O	RX2-	Receiver inverted data output	
22	CML-O	RX2+	Receiver non-inverted data output	
23		GND	Module Ground	1
24	CML-O	RX4-	Receiver inverted data output	
25	CML-O	RX4+	Receiver non-inverted data output	
26		GND	Module Ground	1
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND	
28	LVTTL-O	IntL	Interrupt output, should be pulled up on host board	2
29		VCCT _x	+3.3v Transmitter Power Supply	
30		VCC1	+3.3v Power Supply	
31	LVTTL-I	LPM _o de	Low Power Mode	2
32		GND	Module Ground	1
33	CML-I	Tx3+	Transmitter non-inverted data input	
34	CML-I	Tx3-	Transmitter inverted data input	
35		GND	Module Ground	1
36	CML-I	Tx1+	Transmitter non-inverted data input	
37	CML-I	Tx1-	Transmitter inverted data input	
38		GND	Module Ground	1

Notes:

1. Module circuit ground is isolated from module chassis ground within the module.

2. Open collector; should be pulled up with 4.7k – 10k ohms on host board to a voltage between 3.15V and 3.6V.

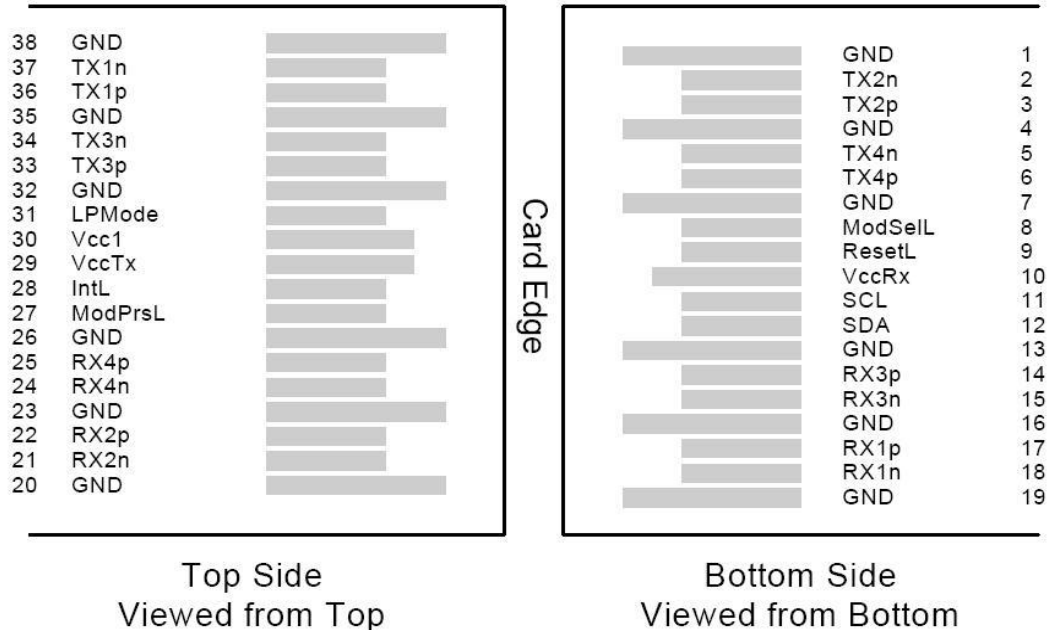


Figure 2. Electrical Pin-out Details

ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is “High”, the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMODE_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_{Reset_init}) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_{init}) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_{init}) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMODE Pin

Gigalight QSFP28 PSM4 operate in the low power mode (less than 1.5 W power consumption). This pin active high will decrease power consumption to less than 1W.

ModPrsL Pin

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted “Low” when the module is inserted and deasserted “High” when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When “Low”, it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure3.

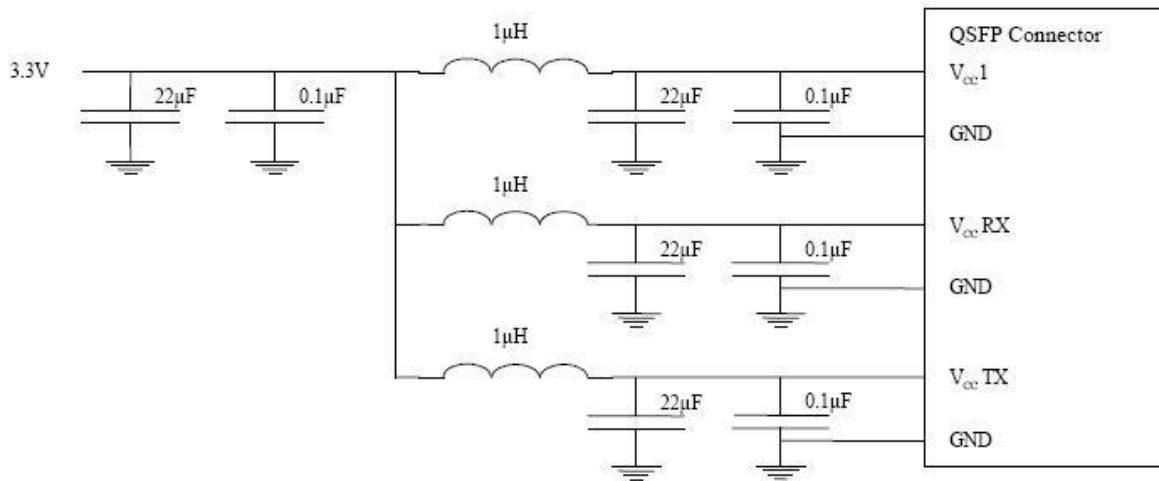


Figure3. Host Board Power Supply Filtering

Optical Interface Lanes and Assignment

The 12 fiber MPO optical lane assignments are shown in Figure 4. The four transmit and four receive optical lanes of PSM4 shall occupy the positions depicted in Figure 8 with looking into the MDI receptacle with the connector keyway feature on top. The interface contains eight active lanes within twelve total positions. The central 4 fibers may be physically present.

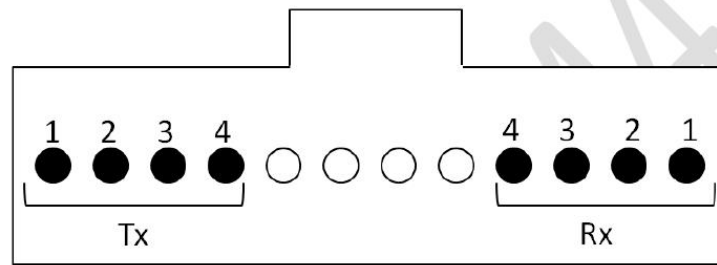


Figure 4. Optical Receptacle and Channel Orientation

DIAGNOSTIC MONITORING INTERFACE (OPTIONAL)

Digital diagnostics monitoring function is available on all Gigalight QSFP28 PSM4. A 2-wire serial interface provides user to contact with module.

The structure of the memory is shown in Figure 5. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function.

The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL, has been asserted, the host can read out the flag field to determine the affected channel and type of flag.

2-wire serial address, 1010000x (A0h)*

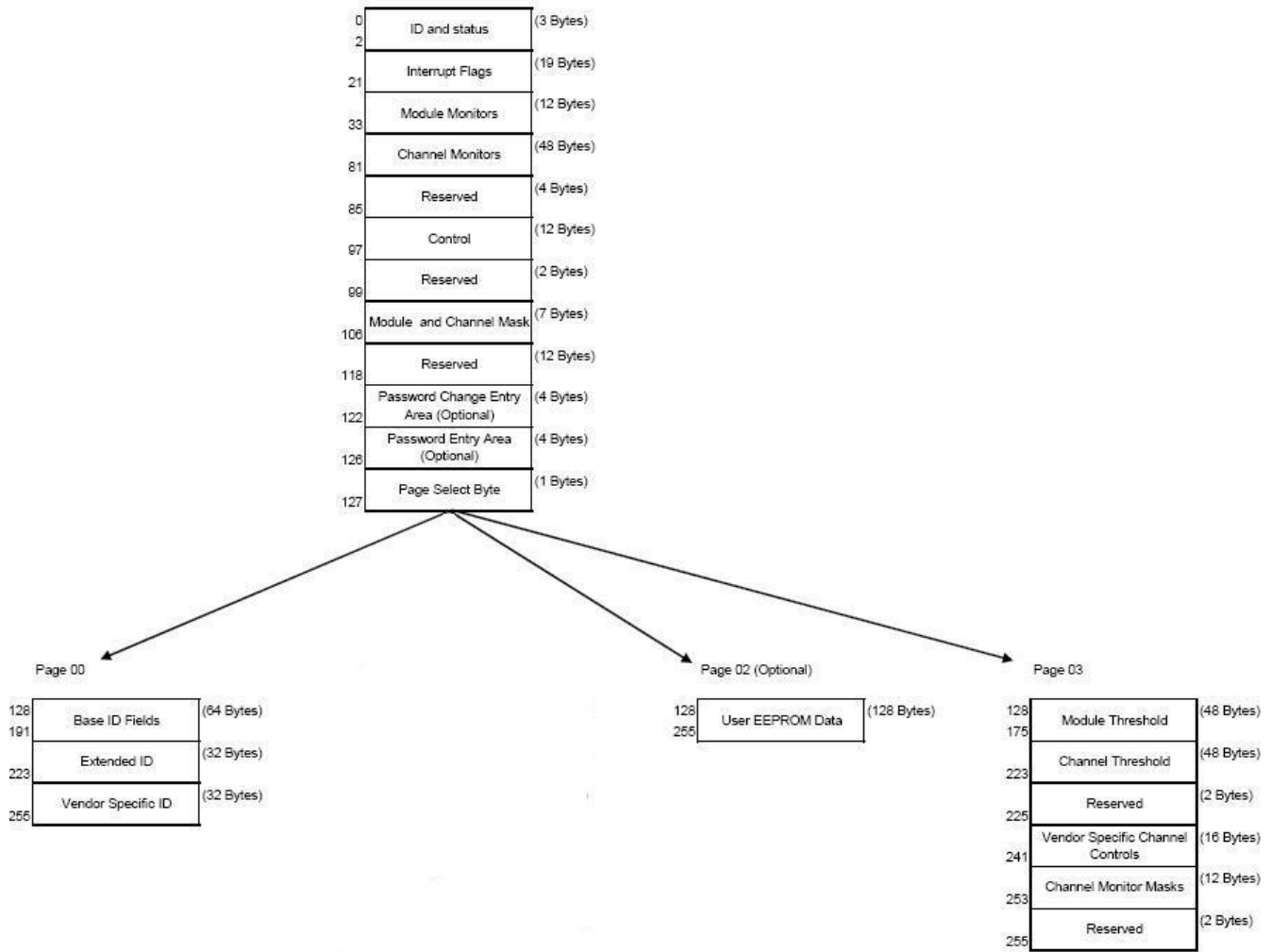


Figure5. QSFP Memory Map

Byte Address	Description	Type
0	Identifier (1 Byte)	Read Only
1-2	Status (2 Bytes)	Read Only
3-21	Interrupt Flags (31 Bytes)	Read Only
22-33	Module Monitors (12 Bytes)	Read Only
34-81	Channel Monitors (48 Bytes)	Read Only
82-85	Reserved (4 Bytes)	Read Only
86-97	Control (12 Bytes)	Read/Write
98-99	Reserved (2 Bytes)	Read/Write
100-106	Module and Channel Masks (7 Bytes)	Read/Write
107-118	Reserved (12 Bytes)	Read/Write
119-122	Reserved (4 Bytes)	Read/Write
123-126	Reserved (4 Bytes)	Read/Write
127	Page Select Byte	Read/Write

Figure6. Low Memory Map

Byte Address	Description	Type
128-175	Module Thresholds (48 Bytes)	Read Only
176-223	Reserved (48 Bytes)	Read Only
224-225	Reserved (2 Bytes)	Read Only
226-239	Reserved (14 Bytes)	Read/Write
240-241	Channel Controls (2 Bytes)	Read/Write
242-253	Reserved (12 Bytes)	Read/Write
254-255	Reserved (2 Bytes)	Read/Write

Figure7. Page 03 Memory Map

Address	Name	Description
128	Identifier (1 Byte)	Identifier Type of serial transceiver
129	Ext. Identifier (1 Byte)	Extended identifier of serial transceiver
130	Connector (1 Byte)	Code for connector type
131-138	Transceiver (8 Bytes)	Code for electronic compatibility or optical compatibility
139	Encoding (1 Byte)	Code for serial encoding algorithm
140	BR, nominal (1 Byte)	Nominal bit rate, units of 100 Mbits/s
141	Extended RateSelect Compliance (1 Byte)	Tags for Extended RateSelect compliance
142	Length SMF (1 Byte)	Link length supported for SM fiber in km
143	Length E-50 μm (1 Byte)	Link length supported for EBW 50/125 μm fiber, units of 2 m
144	Length 50 μm (1 Byte)	Link length supported for 50/125 μm fiber, units of 1 m
145	Length 62.5 μm (1 Byte)	Link length supported for 62.5/125 μm fiber, units of 1 m
146	Length copper (1 Byte)	Link length supported for copper, units of 1 m
147	Device Tech (1 Byte)	Device technology
148-163	Vendor name (16 Bytes)	QSFP vendor name (ASCII)
164	Extended Transceiver (1 Byte)	Extended Transceiver Codes for InfiniBand [†]
165-167	Vendor OUI (3 Bytes)	QSFP vendor IEEE vendor company ID
168-183	Vendor PN (16 Bytes)	Part number provided by QSFP vendor (ASCII)
184-185	Vendor rev (2 Bytes)	Revision level for part number provided by vendor (ASCII)
186-187	Wavelength (2 Bytes)	Nominal laser wavelength (Wavelength = value / 20 in nm)
188-189	Wavelength Tolerance (2 Bytes)	Guaranteed range of laser wavelength (+/- value) from Nominal wavelength (Wavelength Tol. = value / 200 in nm)
190	Max Case Temp (1 Byte)	Maximum Case Temperature in Degrees C
191	CC_BASE (1 Byte)	Check code for Base ID fields (addresses 128-190)
192-195	Options (4 Bytes)	Rate Select, TX Disable, TX Fault, LOS
196-211	Vendor SN (16 Bytes)	Serial number provided by vendor (ASCII)
212-219	Date code (8 Bytes)	Vendor's manufacturing date code
220	Diagnostic Monitoring Type (1 Byte)	Indicates which type of diagnostic monitoring is implemented
221	Enhanced Options (1 Byte)	Indicates which optional enhanced features are implemented
222	Reserved (1 Byte)	Reserved
223	CC_EXT	Check code for the Extended ID Fields (addresses 192-222)
224-255	Vendor Specific (32 Bytes)	Vendor Specific EEPROM

Figure8. Page 00 Memory Map

Page02 is User EEPROM and its format decided by user.

The detail description of low memory and page00.page03 upper memory please see SFF-8436 and SFF-8636 document.

SFF-8636 definiens

TX AND RX CDR LOL indicator (Byte 5)

5	7	L-Tx4 LOL	Latched TX CDR LOL indicator, ch 4	0	0	0	0
	6	L-Tx3 LOL	Latched TX CDR LOL indicator, ch 3	0	0	0	0
	5	L-Tx2 LOL	Latched TX CDR LOL indicator, ch 2	0	0	0	0
	4	L-Tx1 LOL	Latched TX CDR LOL indicator, ch 1	0	0	0	0
	3	L-Rx4 LOL	Latched RX CDR LOL indicator, ch 4	0	0	0	0
	2	L-Rx3 LOL	Latched RX CDR LOL indicator, ch 3	0	0	0	0
	1	L-Rx2 LOL	Latched RX CDR LOL indicator, ch 2	0	0	0	0
	0	L-Rx1 LOL	Latched RX CDR LOL indicator, ch 1	0	0	0	0

TX AND RX CDR BYPASS CONTROL (Byte 98)

98	7	Tx4_CDR_control	Channel 4 TX CDR Control (1b = CDR on, 0b = CDR off)	0	0	0	0
	6	Tx3_CDR_control	Channel 3 TX CDR Control (1b = CDR on, 0b = CDR off)	0	0	0	0
	5	Tx2_CDR_control	Channel 2 TX CDR Control (1b = CDR on, 0b = CDR off)	0	0	0	0
	4	Tx1_CDR_control	Channel 1 TX CDR Control (1b = CDR on, 0b = CDR off)	0	0	0	0
	3	Rx4_CDR_control	Channel 4 RX CDR Control (1b = CDR on, 0b = CDR off)	0	0	0	0
	2	Rx3_CDR_control	Channel 3 RX CDR Control (1b = CDR on, 0b = CDR off)	0	0	0	0
	1	Rx2_CDR_control	Channel 2 RX CDR Control (1b = CDR on, 0b = CDR off)	0	0	0	0
	0	Rx1_CDR_control	Channel 1 RX CDR Control (1b = CDR on, 0b = CDR off)	0	0	0	0

TABLE 6-33 OUTPUT DIFFERENTIAL AMPLITUDE CONTROL (PAGE 03H BYTES 238-239)

Value	Receiver Output Amplitude No Output Equalization	
	Nominal	Units
1xxx b	Reserved	
0111 b	Reserved	mV(P-P)
0110 b	Reserved	mV(P-P)
0101 b	Reserved	mV(P-P)
0100 b	Reserved	mV(P-P)
0011 b	600-1200	mV(P-P)
0010 b	400-800	mV(P-P)
0001 b	300-600	mV(P-P)
0000 b	100-400	mV(P-P)

TABLE 6-34 INPUT EQUALIZATION (PAGE 03H BYTES 234-235)

Value	Transmitter Input Equalization	
	Nominal	Units
11xx b	Reserved	
1011 b	Reserved	
1010 b	10	dB
1001 b	9	dB
1000 b	8	dB
0111 b	7	dB
0110 b	6	dB
0101 b	5	dB
0100 b	4	dB
0011 b	3	dB
0010 b	2	dB
0001 b	1	dB
0000 b	0	No EQ

TABLE 6-35 OUTPUT EMPHASIS CONTROL (PAGE 03H BYTES 236-237)

Value	Receiver Output Emphasis At nominal Output Amplitude	
	Nominal	Units
1xxx b	Reserved	
0111 b	7	dB
0110 b	6	dB
0101 b	5	dB
0100 b	4	dB
0011 b	3	dB
0010 b	2	dB
0001 b	1	dB
0000 b	0	No Emphasis

Timing for Soft Control and Status Functions

Parameter	Symbol	Max	Unit	Conditions
Initialization Time	t_init	2000	ms	Time from power on ¹ , hot plug or rising edge of Reset until the module is fully functional ²
Reset Init Assert Time	t_reset_init	2	μs	A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin.
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on ¹ until module responds to data transmission over the 2-wire serial bus
Monitor Data Ready Time	t_data	2000	ms	Time from power on ¹ to data not ready, bit 0 of Byte 2, deasserted and IntL asserted
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional ²
LPMODE Assert Time	ton_LPMODE	100	μs	Time from assertion of LPMODE (Vin:LPMODE = Vih) until module power consumption enters lower Power Level
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL until Vout:IntL = Vol
IntL Deassert Time	toff_IntL	500	μs	Time from clear on read ³ operation of associated flag until Vout:IntL = Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set and IntL asserted
Tx Fault Assert Time	ton_Txfault	200	ms	Time from Tx Fault state to Tx Fault bit set and IntL asserted
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted
Mask Assert Time	ton_mask	100	ms	Time from mask bit set ⁴ until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask	100	ms	Time from mask bit cleared ⁴ until associated IntL operation resumes
ModSelL Assert Time	ton_ModSelL	100	μs	Time from assertion of ModSelL until module responds to data transmission over the 2-wire serial bus

ModSelL Deassert Time	toff_ModSelL	100	μs	Time from deassertion of ModSelL until the module does not respond to data transmission over the 2-wire serial bus
Power_override or Power-set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set ⁴ until module power consumption enters lower Power Level
Power_override or Power-set Deassert Time	toff_Pdown	300	ms	Time from P_Down bit cleared ⁴ until the module is fully functional ³

Note:

1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.
2. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 deasserted.
3. Measured from falling clock edge after stop bit of read transaction.
4. Measured from falling clock edge after stop bit of write transaction.

Mechanical Dimensions

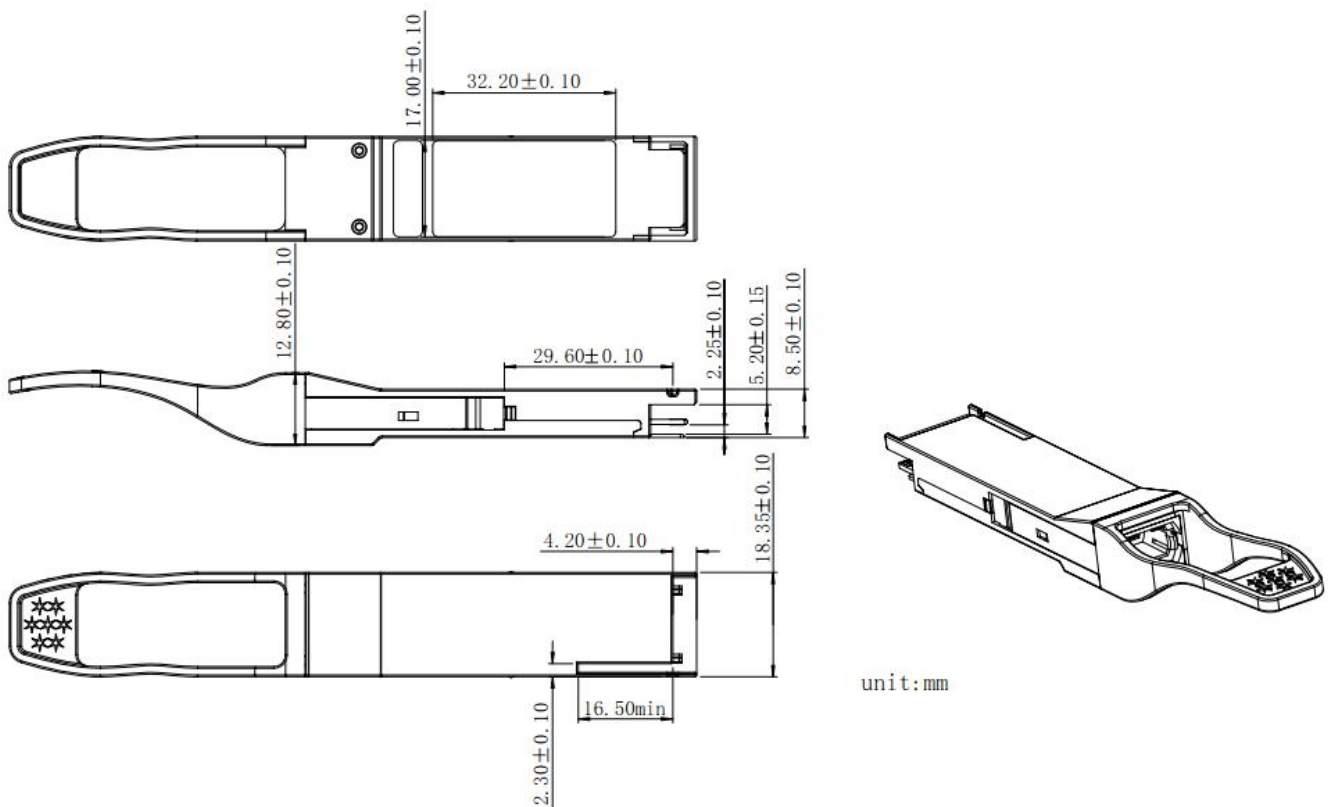
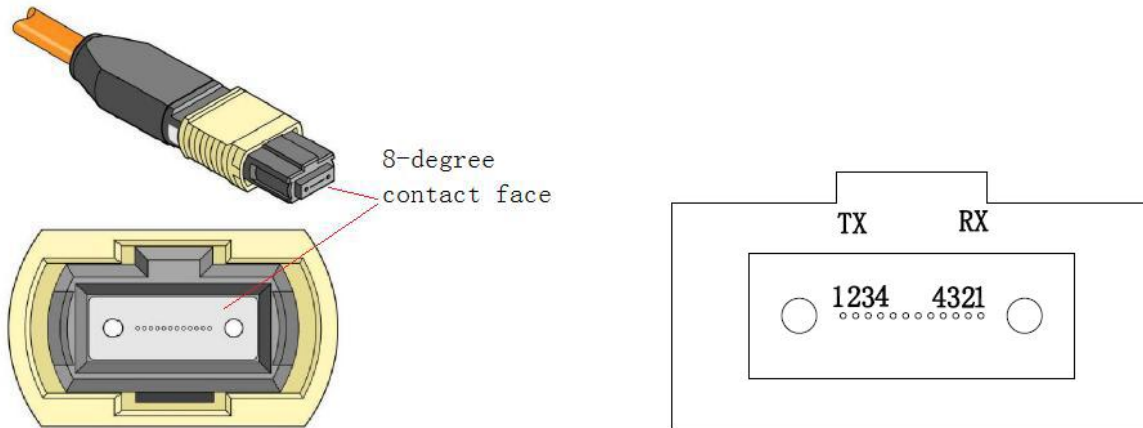


Figure9. Mechanical Specifications



Female MPO(APC 8-degree) connector for this module

Regulatory Compliance

Gigalight GQS-Dxx101-124C QSFP28 transceivers are Class 1 Laser Products. They meet the requirements of the following standards:

Feature	Standard
Laser Safety	IEC 60825-1:2014 (3 rd Edition) IEC 60825-2:2004/AMD2:2010 EN 60825-1-2014 EN 60825-2:2004+A1+A2
Electrical Safety	EN 62368-1: 2014 IEC 62368-1:2014 UL 62368-1:2014
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863
CE EMC	EN55032: 2015 EN55035: 2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B ANSI C63.4-2014

References

1. SFF-8436 QSFP+
2. 100G PSM4 MSA

⚠ CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering information

Part Number	Product Description
GQS-Dxx101-124C	100Gb/s QSFP28 PSM4 C-band DWDM, MPO Connector, reach 120km on G.652 , 0~70°C

Important Notice

Performance figures, data and any illustrative material provided in this data sheet are typical and must be specifically confirmed in writing by Gigalight before they become applicable to any particular order or contract. In accordance with the Gigalight policy of continuous improvement specifications may change without notice.

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Official Site: www.gigalight.com

Revision History

Revision	Date	Description
V0	Nov-6-2023	Advance Release.