

400G QSFP112 - 400G OSFP-RHS AOC Optical Transceiver Module

P/N: GQSO-MDO401-XXXC

Features

- ✓ Hot-plug OSFP-RHS and QSFP112 form factor
- ✓ Transmission data rate up to 106.25G per channel
- ✓ 4x106.25Gbps PAM4 transmitter and PAM4 receiver
- ✓ 4 channels 850nm VCSEL array (both End)
- ✓ 4 channels PIN photo detector array (both End)
- ✓ Power consumption <8W
- ✓ Compliant to OSFP&QSFP112 MSA and CMIS4.0
- ✓ Maximum link length of 30m on OM3 Multimode Fiber (MMF) and 50m on OM4 MMF with FEC
- ✓ Built-in digital diagnostic functions
- ✓ Operating case temperature 0°C to +70°C
- ✓ 3.3V power supply voltage
- ✓ RoHS compliant(lead free)

Applications

- ✓ IEEE 802.3db 400GBASE-VR4 Ethernet (PAM4)
- ✓ The transceiver is designed for Ethernet, Telecom and Infiniband use cases.

Description

Gigalight's GQSO-MDO401-XXXC MMF Active Optical Cable is used in 4 X 100Gigabit Ethernet links over OM3/OM4 multimode fiber. The OSFP-RHS port has integrate 4 independent transmit and receive channels, each capable of 106.25Gb/s PAM4 operation for an aggregate data rate of 425Gb/s, while the QSFP112 port has integrate 4 independent transmit and receive channels and uses QSFP112 MSA, which provides increased port density and total system cost savings for switches and routers, etc. It is compliant with IEEE 802.3db, IEEE 802.3ck and OSFP&QSFP112 MSA.

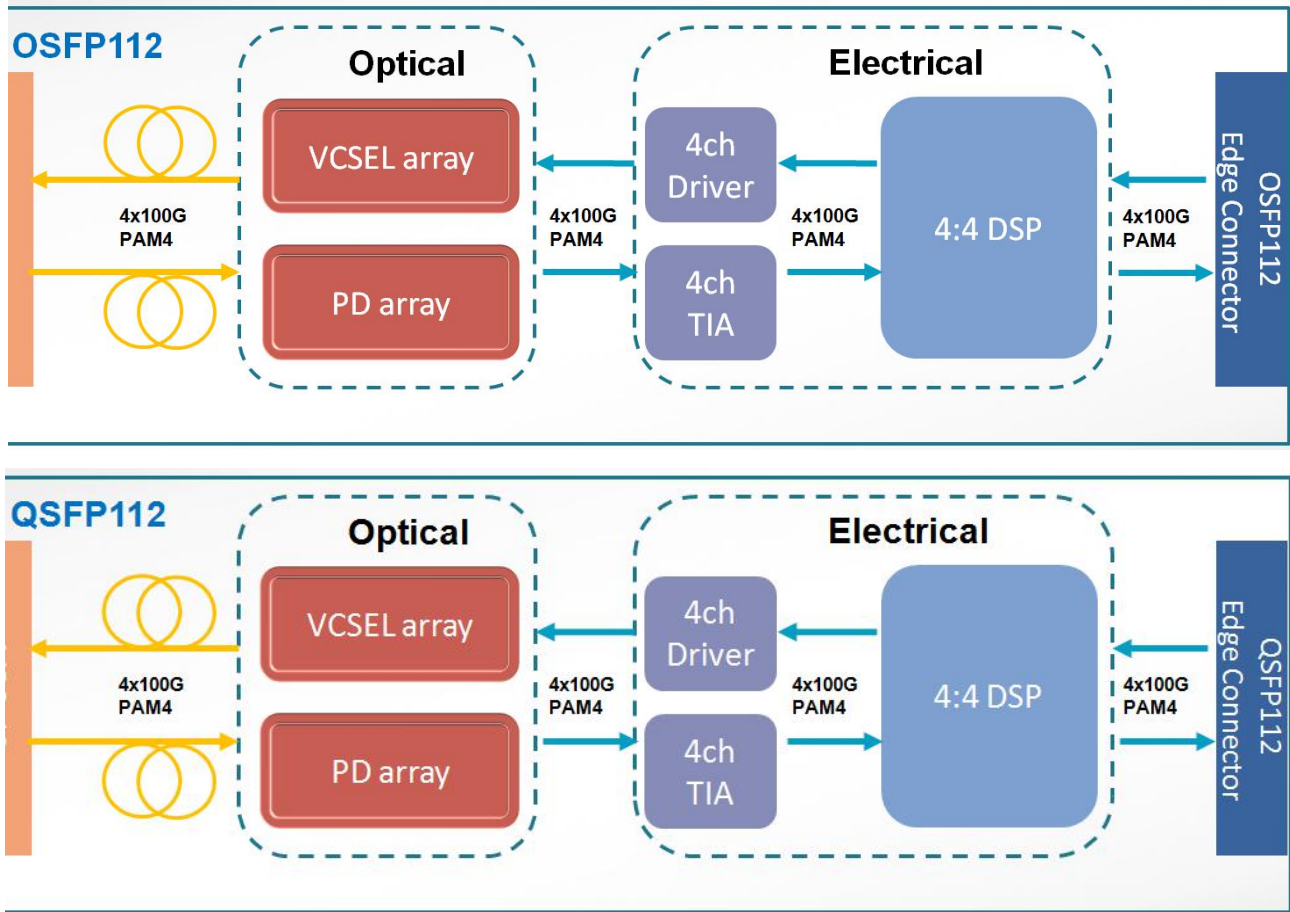


Figure1. Module Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.3	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-20	85	°C
Case Operating Temperature	Top	0	70	°C
Humidity(non-condensing)	Rh	5	85	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case temperature	Tca	0		70	°C
Data Rate Per Lane			106.25		Gbps
Humidity	Rh	5		85	%
Power Dissipation	Pm		7.5	8	W

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential input impedance	Z _{in}	90	100	110	ohm
Differential Output impedance	Z _{out}	90	100	110	ohm
Differential input voltage amplitude	ΔV _{in}	400		900	mVp-p
Differential output voltage	ΔV _{out}			850	mVp-p
Bit Error Rate	BER			2.4E-4	-
Input Logic Level High	V _{IH}	2.0		V _{cc}	V
Input Logic Level Low	V _{IL}	0		0.8	V
Output Logic Level High	V _{OH}	V _{cc} -0.5		V _{cc}	V
Output Logic Level Low	V _{OL}	0		0.4	V
Input Logic Level High	V _{IH}	2.0		V _{cc}	V

Note:

1. BER=2.4E-4; PRBS31Q@53.125GBd. Pre-FEC
2. Differential input voltage amplitude is measured between TxnP and TxnN.
3. Differential output voltage amplitude is measured between RxnP and RxnN.

Optical Characteristics

Table 3 - Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Centre Wavelength	λ _c	842	850	948	nm	-
RMS spectral width	Δλ	-	-	0.65	nm	-
Average launch power, each lane	P _{out}	-4.6	-	5.5	dBm	-
Optical Modulation Amplitude (OMA _{outer}), each lane	OMA	-2.6		4	dBm	-
Transmitter and dispersion eye closure for PAM4(TDECQ),each lane	TDECQ			4.4	dB	
Extinction Ratio	ER	2.5	-	-	dB	-

Average launch power of OFF transmitter, each lane				-30	dB	-
Receiver						
Centre Wavelength	λ_c	842	850	948	nm	-
Receiver Sensitivity in OMAout	RXsen			max (-4.4, TECQ-6.2)	dBm	1
Stressed Receiver Sensitivity in OMAout	SRS			-1.8	dBm	2
Maximum Average power at receiver , each lane input, each lane				5.5	dBm	-
Minimum Average power at receiver , each lane		-6.3			dBm	
Receiver Reflectance				-15	dB	-
LOS Assert	LOSA	-15		-8.5	dBm	-
LOS De-Assert	LOSD			-6.5	dBm	-
LOS Hysteresis	LOSH	0.5			dB	-

Note:

1. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC.
2. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Digital Diagnostic Specification

Parameter	Symbol	Min	Typical	Max	Units	Notes
Transceiver Case Temperature	DMI_Temp	-3		+3	°C	Over operating temp
Supply voltage monitor absolute error	DMI_VCC	-0.1		0.1	V	Full operating range
Channel RX power monitor absolute error	DMI_RX	-2		+2	dB	Per channel
Channel Bias current monitor	DMI_Ibias	-10%		+10%	mA	Per channel
Channel TX power monitor absolute error	DMI_TX	-2		+2	dB	Per channel

Pin Description

Electrical Pin Definition(OSFP)

Pin	Symbol	Description	Logic	Direction
1	GND	Ground		
2	TX2p	Transmitter Data Non- Inverted	CML-I	Input from Host
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host
4	GND	Ground		
5	TX4p	Transmitter Data Non- Inverted	CML-I	Input from Host
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host
7	GND	Ground		
8	TX6p	Transmitter Data Non- Inverted	CML-I	Input from Host
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host
10	GND	Ground		
11	TX8p	Transmitter Data Non- Inverted	CML-I	Input from Host
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host
13	GND	Ground		
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi- directional
15	VCC	+3.3V Power		Power from Host
16	VCC	+3.3V Power		Power from Host
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi- directional
18	GND	Ground		
19	RX7n	Receiver Data Inverted	CML-O	Output to Host
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host
21	GND	Ground		
22	RX5n	Receiver Data Inverted	CML-O	Output to Host
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host
24	GND	Ground		
25	RX3n	Receiver Data Inverted	CML-O	Output to Host
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host
27	GND	Ground		
28	RX1n	Receiver Data Inverted	CML-O	Output to Host
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host
30	GND	Ground		
31	GND	Ground		
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host
33	RX2n	Receiver Data Inverted	CML-O	Output to Host

34	GND	Ground		
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host
36	RX4n	Receiver Data Inverted	CML-O	Output to Host
37	GND	Ground		
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host
39	RX6n	Receiver Data Inverted	CML-O	Output to Host
40	GND	Ground		
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host
42	RX8n	Receiver Data Inverted	CML-O	Output to Host
43	GND	Ground		
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi- directional
45	VCC	+3.3V Power		Power from Host
46	VCC	+3.3V Power		Power from Host
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi- directional
48	GND	Ground		
49	TX7n	Transmitter Data Inverted	CML-I	Input
50	TX7p	Transmitter Data Non- Inverted	CML-I	Input from Host
51	GND	Ground		
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host
53	TX5p	Transmitter Data Non- Inverted	CML-I	Input from Host
54	GND	Ground		
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host
56	TX3p	Transmitter Data Non- Inverted	CML-I	Input from Host
57	GND	Ground		
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host
59	TX1p	Transmitter Data Non- Inverted	CML-I	Input from Host
60	GND	Ground		

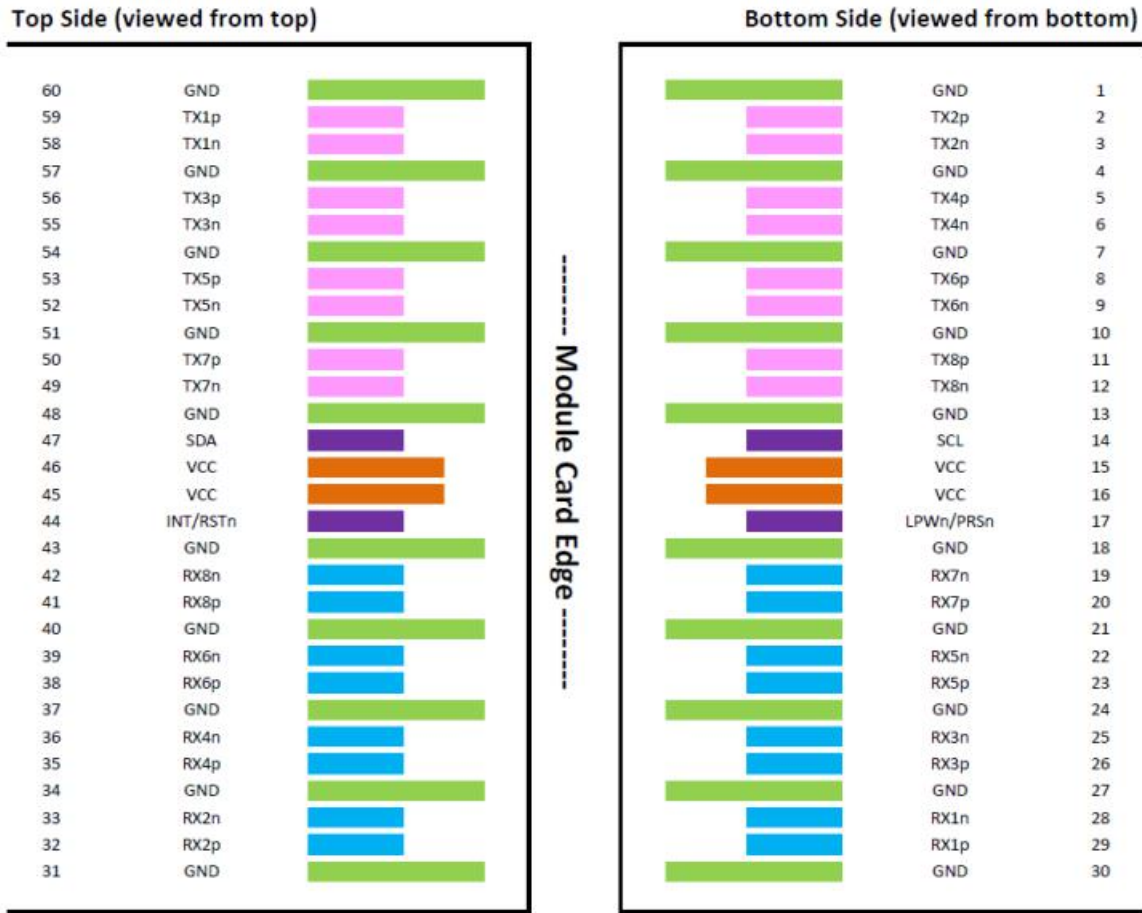


Figure2. Electrical Pin-out Details

OSFP Control pins

Name	Function	Description
LPWn/PRSn	Input/output	Multi-level signal for low power control from host to module and module presence indication from module to host. This signal requires the circuit as described in the OSFP Specification.
INT/RSTn	Input, /output	Multi-level signal for interrupt request from module to host and reset control from host to module. This signal requires the circuit as described in the OSFP Specification.

Name	Function	Description
SCL	BiDir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host.
SDA	Bidir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.

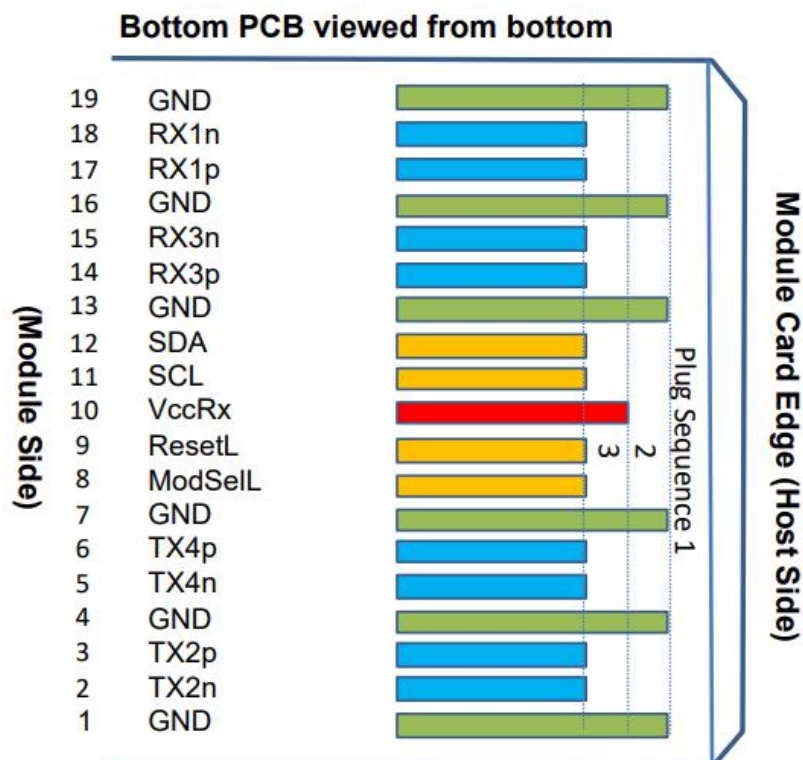
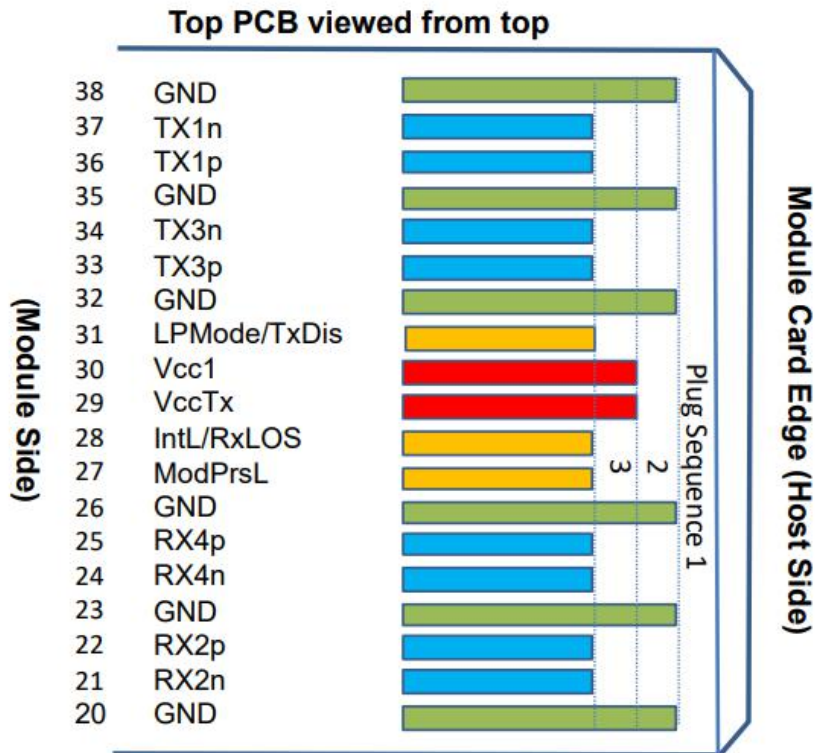
Electrical Pin Definition(QSFP112)

Pad	Logic	Symbol	Description	Plug Sequence ⁴	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply Receiver	2	2
11	LVC MOS-I/O	SCL	TWI serial interface clock	3	
12	LVC MOS-I/O	SDA	TWI serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL/ RxLOS	Interrupt/optional RxLOS	3	
29		VccTx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPM mode/ TxDis	Low Power mode/optional TX Disable	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Note 1: QSFP112 uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector Gnd contact is rated for a maximum current of 500 mA.

Note 2: VccRx, Vcc1, and VccTx shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector are listed in Table 13. For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a maximum current of 1500 mA.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1, 2, and 3 see Figure 14 for pad locations.



Classic

QSFP+/QSFP28/QSFP112 Pads

Figure 3. Electrical Pin-out Details

ModSelL Pin

The ModSelL is an input signal that shall be pulled to Vcc in the QSFP112 modules. When held low by the host, the module responds to TWI serial communication commands. The ModSelL allows the use of multiple QSFP112 modules on a single TWI interface bus. When ModSelL is “High”, the module shall not respond to or acknowledge any TWI interface communication from the host.

In order to avoid conflicts, the host system shall not attempt TWI interface communications within the ModSelL de-assert time after any QSFP112 modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL Pin

The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length ($t_{\text{Reset_init}}$) initiates a complete module reset, returning all user module settings to their default state.

LPMoDe/TxDiS Pin

LPMoDe/TxDiS is a dual-mode input signal from the host operating with active high logic. It shall be pulled towards Vcc in the module. At power-up or after ResetL is deasserted LPMoDe/TxDiS behaves as LPMoDe. If supported, LPMoDe/TxDiS can be configured as TxDiS using the TWI interface except during the execution of a reset.

ModPrsL Pin

ModPrsL shall be pulled up to Vcc Host on the host board and pulled low in the module. The ModPrsL is asserted “Low” when the module is inserted. The ModPrsL is deasserted “High” when the module is physically absent from the host connector due to the pull-up resistor on the host board.

IntL/RxLOSL Pin

IntL/RxLOSL is a dual-mode active-low, open-collector output signal from the module. It shall be pulled up towards Vcc on the host board. At power-up or after ResetL is released to high, IntL/RxLOSL is configured as IntL. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the TWI serial interface. The IntL signal is deasserted “High” after all set interrupt

flags are read. If dual mode operation supported, IntL/RxLOSL can be optionally programmed as RxLOSL using the TWI interface except during the execution of a reset. If the module has no interrupt flags asserted (IntL/RxLOSL is high), there should be no change in IntL/RxLOSL states after the mode change.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure3.

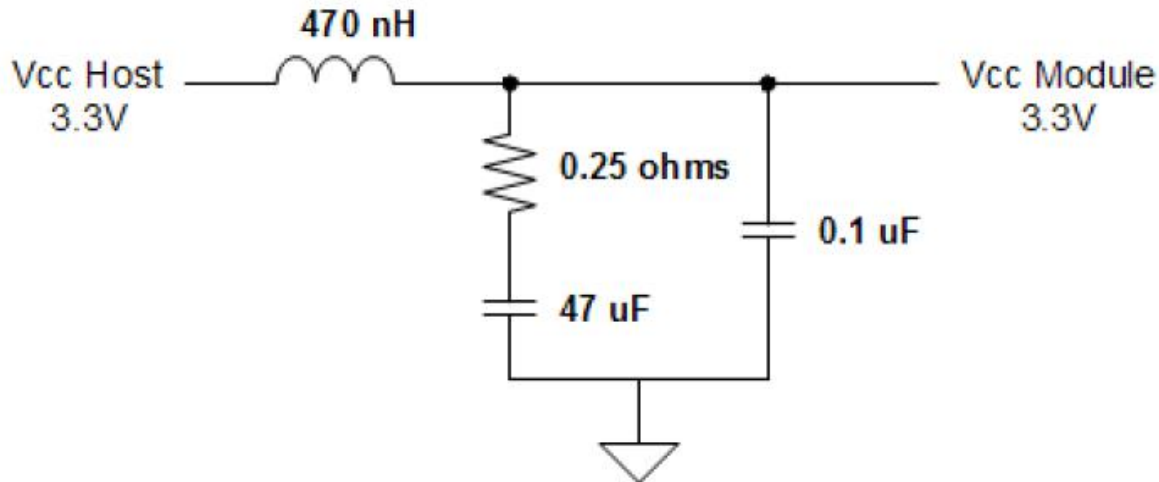


Figure4. OSFP Host Board Power Supply Filtering

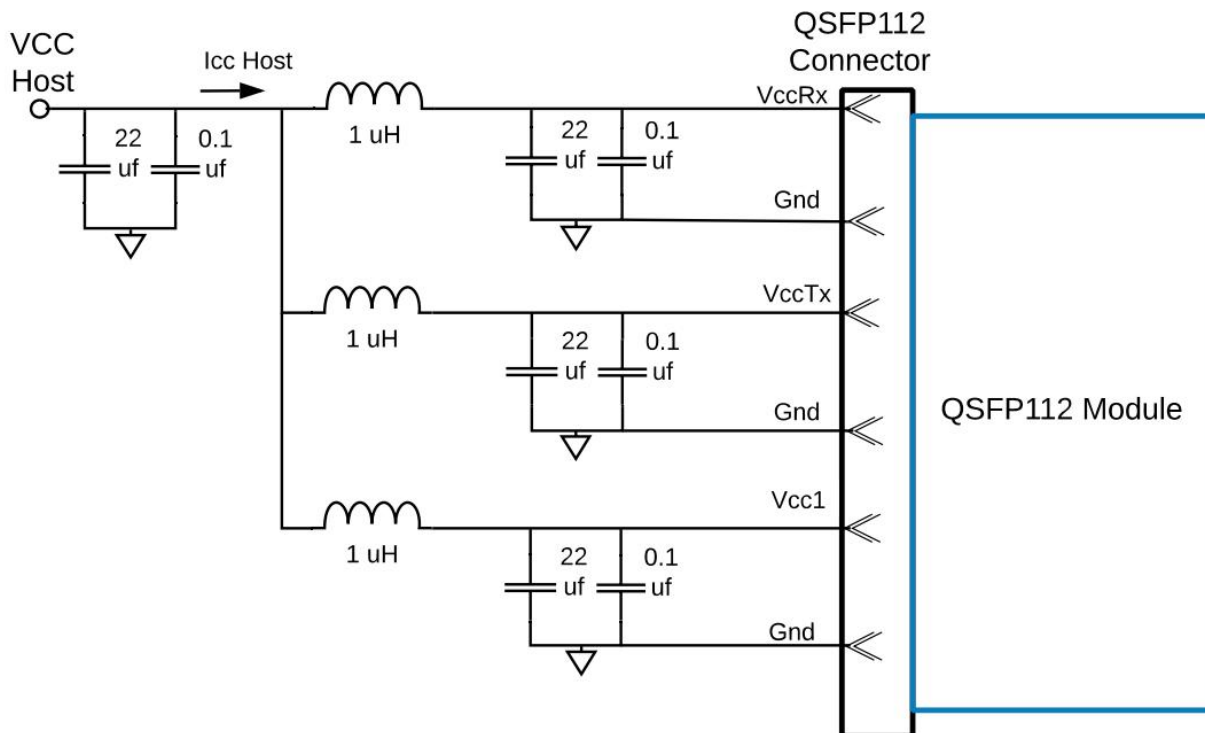


Figure5. Host Board Power Supply Filtering

DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics monitoring function is available on all Gigalight OSFP products. A 2-wire serial interface provides user to contact with module.

Memory Structure and Mapping

This limits the management memory that can be directly accessed by the host to 256 bytes, which is divided in Lower Memory (addresses 00h through 7Fh) and Upper Memory (addresses 80h through FFh).

A larger addressable management memory is required for all but the most basic modules. This is supported by a structure of 128-byte pages, together with a mechanism for dynamically mapping any of the 128-byte pages from a larger internal management memory space into Upper Memory the host addressable space.

The addressing structure of the additional internal management memory is shown in Figure 4 The management memory inside the module is arranged as a unique and always host accessible address space of 128 bytes (Lower Memory) and as multiple upper address subspaces of 128 bytes each (Pages), only one of which is selected as host visible in Upper Memory. A second level of Page selection is possible for Pages for which several instances exist (e.g. where a bank of pages with the same Page number exists).

This structure supports a flat 256 byte memory for passive copper modules and permits timely access to addresses in the Lower Memory, e.g. Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function in the Lower Page. For more complex modules which require a larger amount of management memory the host needs to use dynamic mapping of the various Pages into the host addressable Upper Memory address space, whenever needed.

Note: The management memory map has been designed largely after the QSFP memory map. This memory map has been changed in order to accommodate 8 electrical lanes and to limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

Supported Pages

A basic 256 byte subset of the Management Memory Map is mandatory for all CMIS compliant devices. Other parts are only available for paged memory modules, or when advertised by the module. See CMIS

V4.0 for details regarding the advertisement of supported management memory spaces.

In particular, support of the Lower Memory and of Page 00h is required for all modules, including passive copper cables. These pages are therefore always implemented. Additional support for Pages 01h, 02h and bank 0 of Pages 10h and 11h is required for all paged memory modules.

Bank 0 of pages 10h-1Fh, provides lane-specific registers for the first 8 lanes, and each additional bank provides support for additional 8 lanes. Note, however, that the allocation of information over the banks may be page specific and may not to be related to grouping data for 8 lanes.

The structure allows address space expansion for certain types of modules by allocating additional Pages. Moreover, additional banks of pages.

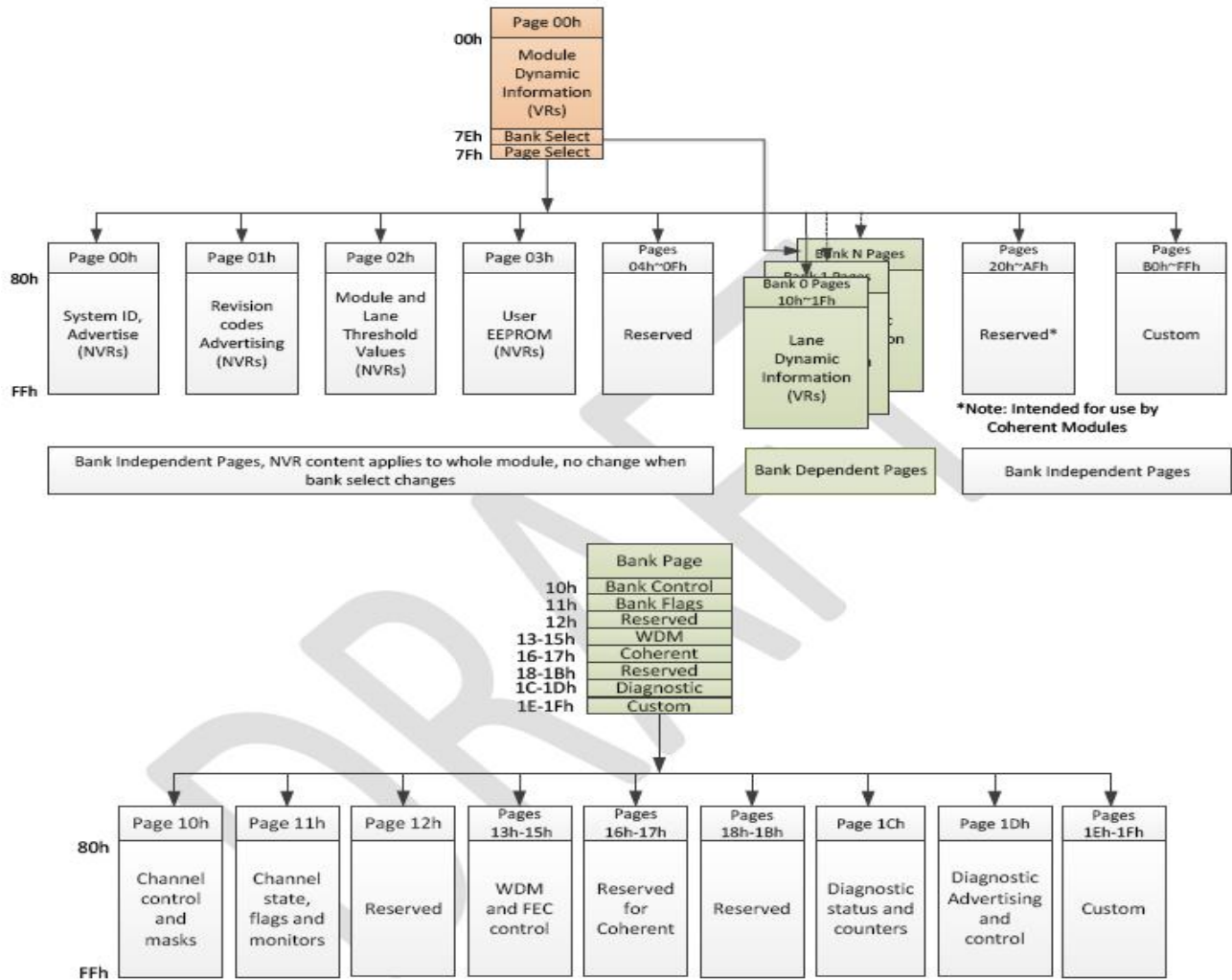


Figure6. Memory Map

Mechanical Dimensions(mm)

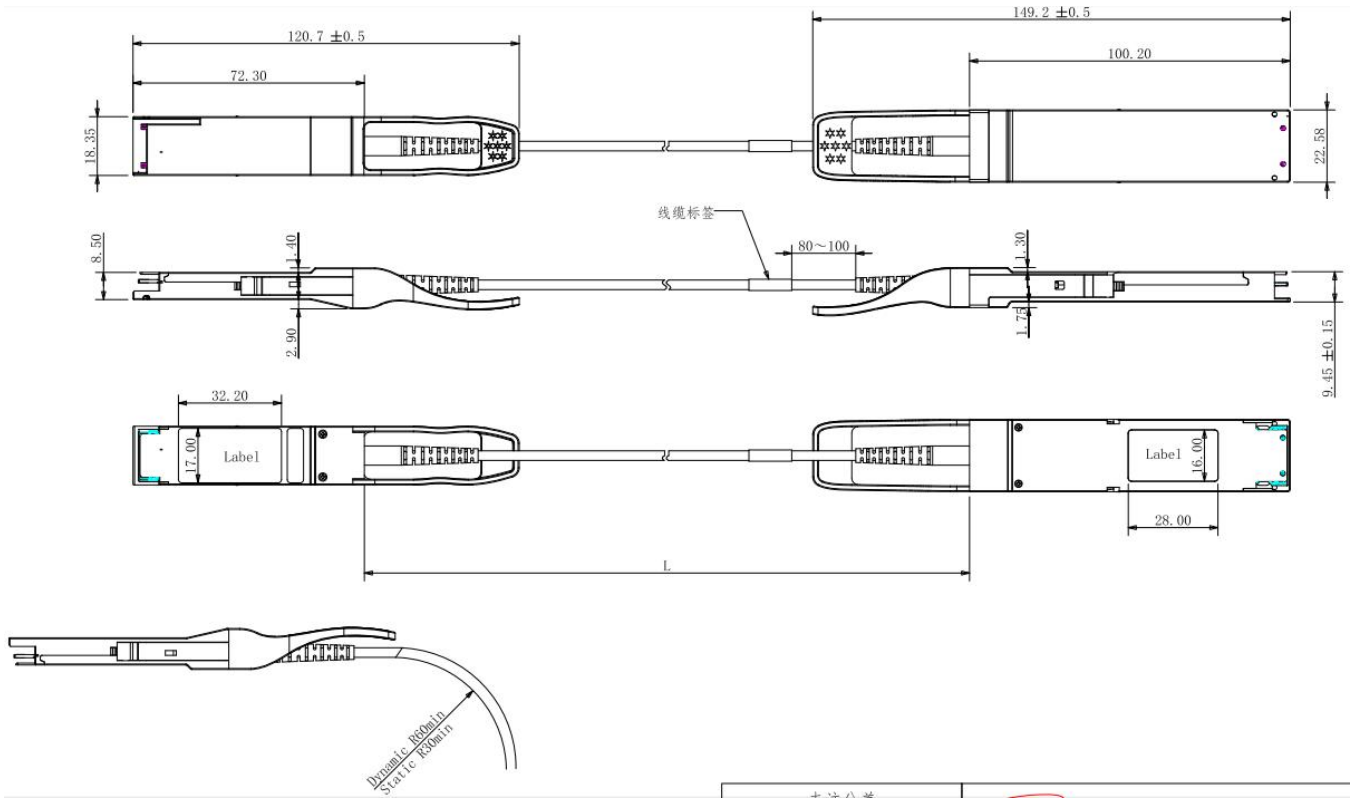


Figure7. Mechanical Specifications

Regulatory Compliance

Gigalight GQSO-MDO401-XXXC transceivers are Class 1 Laser Products. They meet the requirements of the following standards:

Feature	Standard
Laser Safety	IEC 60825-1:2014 (3 rd Edition) IEC 60825-2:2004/AMD2:2010 EN 60825-1:2014 EN 60825-2:2004+A1+A2
Electrical Safety	EN 62368-1: 2014 IEC 62368-1:2014 UL 62368-1:2014
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863
CE EMC	EN55032: 2015 EN55035: 2017 EN61000-3-2:2014 EN61000-3-3:2013

FCC

FCC Part 15, Subpart B
ANSI C63.4-2014

References

1. OSFP MSA&QSFP112 MSA
2. CMIS V4.0
3. IEEE 802.3db 400GBASE-VR4 Ethernet (PAM4)
4. IEEE802.3ck

CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering information

Part Number	Product Description
GQSO-MDO401-XXXC	400G QSFP112 - 400G OSFP-RHS AOC transceiver, 850nm, up to 50m with OM4, XXX: 001-1m, 005-5m, 007-7m, 020-20m, 030-30m, 050-50m

Important Notice

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Revision History

Revision	Date	Description
V0	Jun-6-2024	Advance Release.