# GIGALIGHT 800G QSFPDD DR8 500m Silicon Photonics Transceiver Module

# P/N: GQD-SI801DR8C

## Features

- ✓ QSFPDD MSA and CMIS compliant
- ✓ 8x106.25Gbps(53.125GBd PAM4)electrical interface
- ✓ 8x106.25Gbps(53.125GBd PAM4)optics architecture
- ✓ Power consumption <18.5W
- ✓ Maximum link length of 500m G.652 SMF with KP-FEC
- ✓ MPO-16 receptacles
- ✓ Built-in digital diagnostic functions
- ✓ Operating case temperature 0℃ to +70℃
- ✓ 3.3V power supply voltage
- ✓ RoHS compliant(lead free)

## Applications

- ✓ 800GBASE-DR8
- ✓ Data center network

## Description

The Gigalight GQD-SI801DR8C is a transceiver module designed for 500m optical communication applications, and it is compliant to QSFPDD MSA, IEEE 802.3 protocol. The silicon photonics transceiver is based on a new state-of-the-art silicon photonics (SiPh) platform. It uses SiPh chips that integrate a number of active and passive optoelectronic components, 3D packaging technology and 7nm DSP chips. It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference. The module offers very high functionality and feature integration, accessible via a two-wire serial interface.

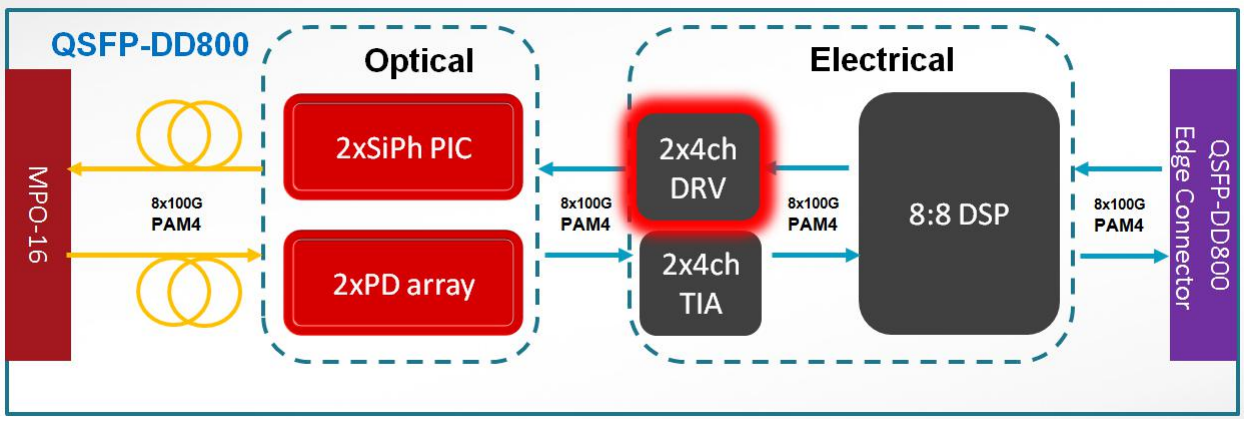


**Figure1. Module Block Diagram**

## Absolute Maximum Ratings

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage | Vcc | -0.3 | 3.6 | V |
| Input Voltage | Vin | -0.3 | Vcc+0.3 | V |
| Storage Temperature | Tst | -40 | 85 | ℃ |
| Case Operating Temperature | Top | 0 | 70 | ℃ |
| Humidity(non-condensing) | Rh | 5 | 95 | % |

## Recommended Operating Conditions

| Parameter | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | Vcc | 3.13 | 3.3 | 3.47 | V |
| Operating Case temperature | Tca | 0 | | 70 | ℃ |
| Data Rate Per Lane | fd | | 106.25 | | Gbit/s |
| Humidity | Rh | 5 | | 85 | % |
| Power Dissipation | Pm | | | 18.5 | W |

## Electrical Specifications

| Parameter | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Differential input impedance | Zin | 90 | 100 | 110 | ohm |

| | | | | | |
|---|---|---|---|---|---|
| Differential Output impedance | Zout | 90 | 100 | 110 | ohm |
| Differential input voltage amplitude | ΔVin | 400 | | 900 | mVp-p |
| Differential output voltage amplitude | ΔVout | | | 850 | mVp-p |
| Bit Error Rate | BER | | | 2.4E-4 | - |
| Input Logic Level High | $V_{IH}$ | 2.0 | | $V_{cc}$ | V |
| Input Logic Level Low | $V_{IL}$ | 0 | | 0.8 | V |
| Output Logic Level High | $V_{OH}$ | $V_{cc}$-0.5 | | $V_{cc}$ | V |
| Output Logic Level Low | $V_{OL}$ | 0 | | 0.4 | V |

**Note：**

1) BER=2.4E-4; PRBS31Q@53.125GBd. Pre-FEC
2) Differential input voltage amplitude is measured between TxnP and TxnN.
3) Differential output voltage amplitude is measured between RxnP and RxnN.

## Optical Characteristics

| Parameter | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| **Transmitter** | | | | | | |
| Centre Wavelength | λc | 1304.5 | | 1317.5 | nm | - |
| Side-mode suppression ratio | SMSR | 30 | - | -- | dB | - |
| Average launch power, each lane | Pout | -2.9 | - | 4.0 | dBm | - |
| Optical Modulation Amplitude(OMA outer), each lane | OMA | -0.8 | - | 4.2 | dBm | - |
| Transmitter and dispersion eye closure for PAM4 (TDECQ),each lane | TDECQ | | | 3.4 | dB | |
| Extinction Ratio | ER | 3.5 | - | - | dB | - |
| Average launch power of OFF transmitter, each lane | | | | -15 | dB | - |
| **Receiver** | | | | | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| Centre Wavelength | λc | 1304.5 | | 1317.5 | nm | - |
| Receiver Sensitivity in OMA outer | RXsen | | | -4.4 | dBm | 1 |
| Average power at receiver , each lane input, each lane | Pin | -5.9 | | 4 | dBm | - |
| Receiver Reflectance | | | | -26 | dB | - |
| LOS Assert | | -14 | -13 | | dBm | - |
| LOS De-Assert | | | -11 | -10 | dBm | - |
| LOS Hysteresis | | 0.5 | | | dB | - |

**Note：**

1) Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC

## Pin Description

Table 1- Pad Function Definition

| Pad | Logic | Symbol | Description | Plug Sequence[4] | Notes |
|---|---|---|---|---|---|
| 1 | | GND | Ground | 1B | 1 |
| 2 | CML-I | Tx2n | Transmitter Inverted Data Input | 3B | |
| 3 | CML-I | Tx2p | Transmitter Non-Inverted Data Input | 3B | |
| 4 | | GND | Ground | 1B | 1 |
| 5 | CML-I | Tx4n | Transmitter Inverted Data Input | 3B | |
| 6 | CML-I | Tx4p | Transmitter Non-Inverted Data Input | 3B | |
| 7 | | GND | Ground | 1B | 1 |
| 8 | LVTTL-I | ModSelL | Module Select | 3B | |
| 9 | LVTTL-I | ResetL | Module Reset | 3B | |
| 10 | | VccRx | +3.3V Power Supply Receiver | 2B | 2 |
| 11 | LVCMOS-I/O | SCL | 2-wire serial interface clock | 3B | |
| 12 | LVCMOS-I/O | SDA | 2-wire serial interface data | 3B | |
| 13 | | GND | Ground | 1B | 1 |
| 14 | CML-O | Rx3p | Receiver Non-Inverted Data Output | 3B | |
| 15 | CML-O | Rx3n | Receiver Inverted Data Output | 3B | |
| 16 | | GND | Ground | 1B | 1 |
| 17 | CML-O | Rx1p | Receiver Non-Inverted Data Output | 3B | |
| 18 | CML-O | Rx1n | Receiver Inverted Data Output | 3B | |
| 19 | | GND | Ground | 1B | 1 |
| 20 | | GND | Ground | 1B | 1 |
| 21 | CML-O | Rx2n | Receiver Inverted Data Output | 3B | |
| 22 | CML-O | Rx2p | Receiver Non-Inverted Data Output | 3B | |
| 23 | | GND | Ground | 1B | 1 |
| 24 | CML-O | Rx4n | Receiver Inverted Data Output | 3B | |
| 25 | CML-O | Rx4p | Receiver Non-Inverted Data Output | 3B | |
| 26 | | GND | Ground | 1B | 1 |
| 27 | LVTTL-O | ModPrsL | Module Present | 3B | |
| 28 | LVTTL-O | IntL | Interrupt | 3B | |
| 29 | | VccTx | +3.3V Power supply transmitter | 2B | 2 |
| 30 | | Vcc1 | +3.3V Power supply | 2B | 2 |
| 31 | LVTTL-I | LPMode | Low Power mode; | 3B | |
| 32 | | GND | Ground | 1B | 1 |
| 33 | CML-I | Tx3p | Transmitter Non-Inverted Data Input | 3B | |
| 34 | CML-I | Tx3n | Transmitter Inverted Data Input | 3B | |
| 35 | | GND | Ground | 1B | 1 |
| 36 | CML-I | Tx1p | Transmitter Non-Inverted Data Input | 3B | |
| 37 | CML-I | Tx1n | Transmitter Inverted Data Input | 3B | |
| 38 | | GND | Ground | 1B | 1 |

| Pad | Logic | Symbol | Description | Plug Sequence[4] | Notes |
|---|---|---|---|---|---|
| 39 | | GND | Ground | 1A | 1 |
| 40 | CML-I | Tx6n | Transmitter Inverted Data Input | 3A | |
| 41 | CML-I | Tx6p | Transmitter Non-Inverted Data Input | 3A | |
| 42 | | GND | Ground | 1A | 1 |
| 43 | CML-I | Tx8n | Transmitter Inverted Data Input | 3A | |
| 44 | CML-I | Tx8p | Transmitter Non-Inverted Data Input | 3A | |
| 45 | | GND | Ground | 1A | 1 |
| 46 | | Reserved | For future use | 3A | 3 |
| 47 | | VS1 | Module Vendor Specific 1 | 3A | 3 |
| 48 | | VccRx1 | 3.3V Power Supply | 2A | 2 |
| 49 | | VS2 | Module Vendor Specific 2 | 3A | 3 |
| 50 | | VS3 | Module Vendor Specific 3 | 3A | 3 |
| 51 | | GND | Ground | 1A | 1 |
| 52 | CML-O | Rx7p | Receiver Non-Inverted Data Output | 3A | |
| 53 | CML-O | Rx7n | Receiver Inverted Data Output | 3A | |
| 54 | | GND | Ground | 1A | 1 |
| 55 | CML-O | Rx5p | Receiver Non-Inverted Data Output | 3A | |
| 56 | CML-O | Rx5n | Receiver Inverted Data Output | 3A | |
| 57 | | GND | Ground | 1A | 1 |
| 58 | | GND | Ground | 1A | 1 |
| 59 | CML-O | Rx6n | Receiver Inverted Data Output | 3A | |
| 60 | CML-O | Rx6p | Receiver Non-Inverted Data Output | 3A | |
| 61 | | GND | Ground | 1A | 1 |
| 62 | CML-O | Rx8n | Receiver Inverted Data Output | 3A | |
| 63 | CML-O | Rx8p | Receiver Non-Inverted Data Output | 3A | |
| 64 | | GND | Ground | 1A | 1 |
| 65 | | NC | No Connect | 3A | 3 |
| 66 | | Reserved | For future use | 3A | 3 |
| 67 | | VccTx1 | 3.3V Power Supply | 2A | 2 |
| 68 | | Vcc2 | 3.3V Power Supply | 2A | 2 |
| 69 | LVTTL-I | ePPS | Precision Time Protocol (PTP) reference clock input | 3A | 3 |
| 70 | | GND | Ground | 1A | 1 |
| 71 | CML-I | Tx7p | Transmitter Non-Inverted Data Input | 3A | |
| 72 | CML-I | Tx7n | Transmitter Inverted Data Input | 3A | |
| 73 | | GND | Ground | 1A | 1 |
| 74 | CML-I | Tx5p | Transmitter Non-Inverted Data Input | 3A | |
| 75 | CML-I | Tx5n | Transmitter Inverted Data Input | 3A | |
| 76 | | GND | Ground | 1A | 1 |

Note 1: QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 7. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

Note 3: All Vendor Specific, Reserved, No Connect and ePPS (if not used) pins may be terminated with 50 Ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A,1B will then occur simultaneously, followed by 2A,2B,followed by 3A,3B.

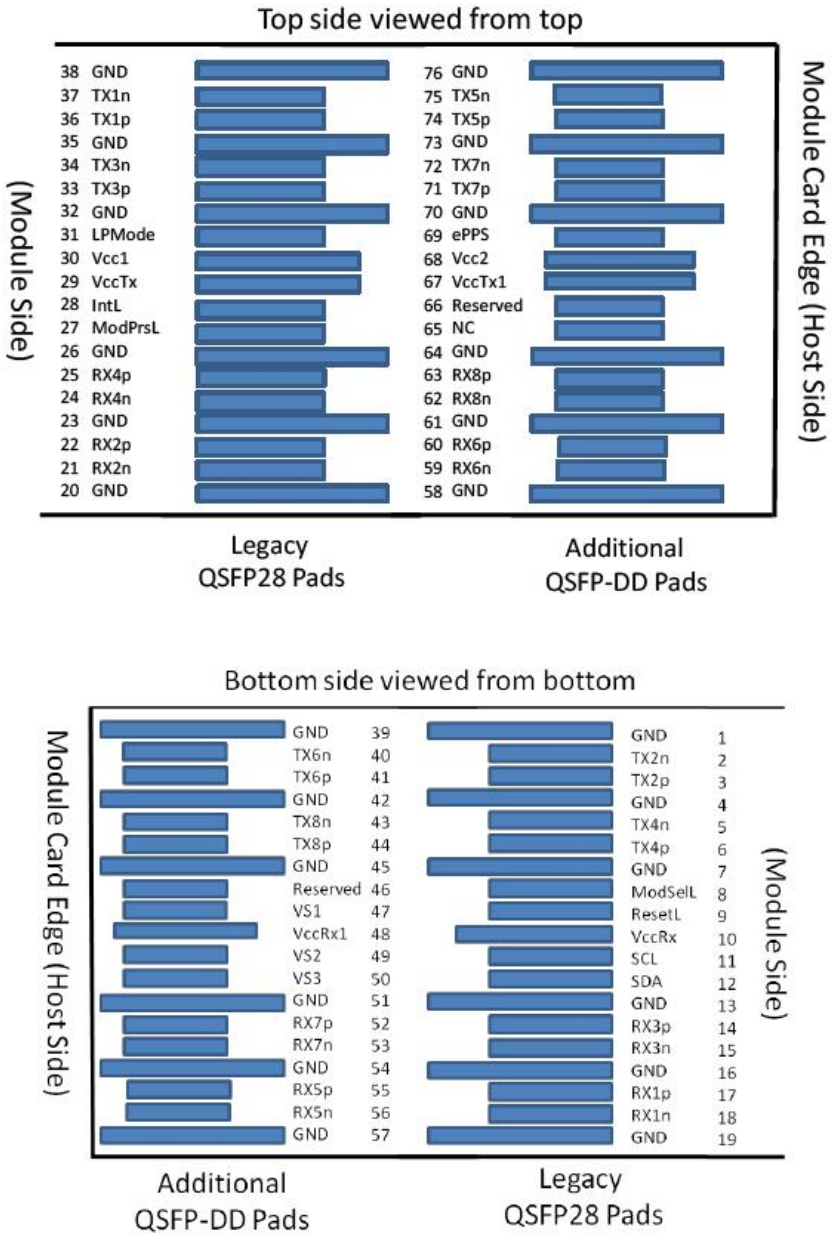


**Figure2. Electrical Pin-out Details**

**ModSelL Pin**

The ModSelL is an input signal that shall be pulled to Vcc in the QSFP-DD module. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When ModSelL is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the

ModSelL de-assert time after any QSFP-DD modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

**ResetL Pin**

The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state.

**LPMode Pin**

LPMode is an input signal. The LPMode signal shall be pulled up to Vcc in the QSFP-DD module. LPMode is used in the control of the module power mode. See CMIS Section 6.3.1.3.

**ModPrsL Pin**

ModPrsL shall be pulled up to Vcc Host on the host board and pulled low in the module. The ModPrsL is asserted “Low” when the module is inserted. The ModPrsL is deasserted “High” when the module is physically absent from the host connector due to the pull-up resistor on the host board.

**IntL Pin**

IntL is an output signal. The IntL signal is an open collector output and shall be pulled to Vcc Host on the host board. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is deasserted “High” after all set interrupt flags are read.

## Power Supply Filtering

The host board should use the power supply filtering shown in Figure3.

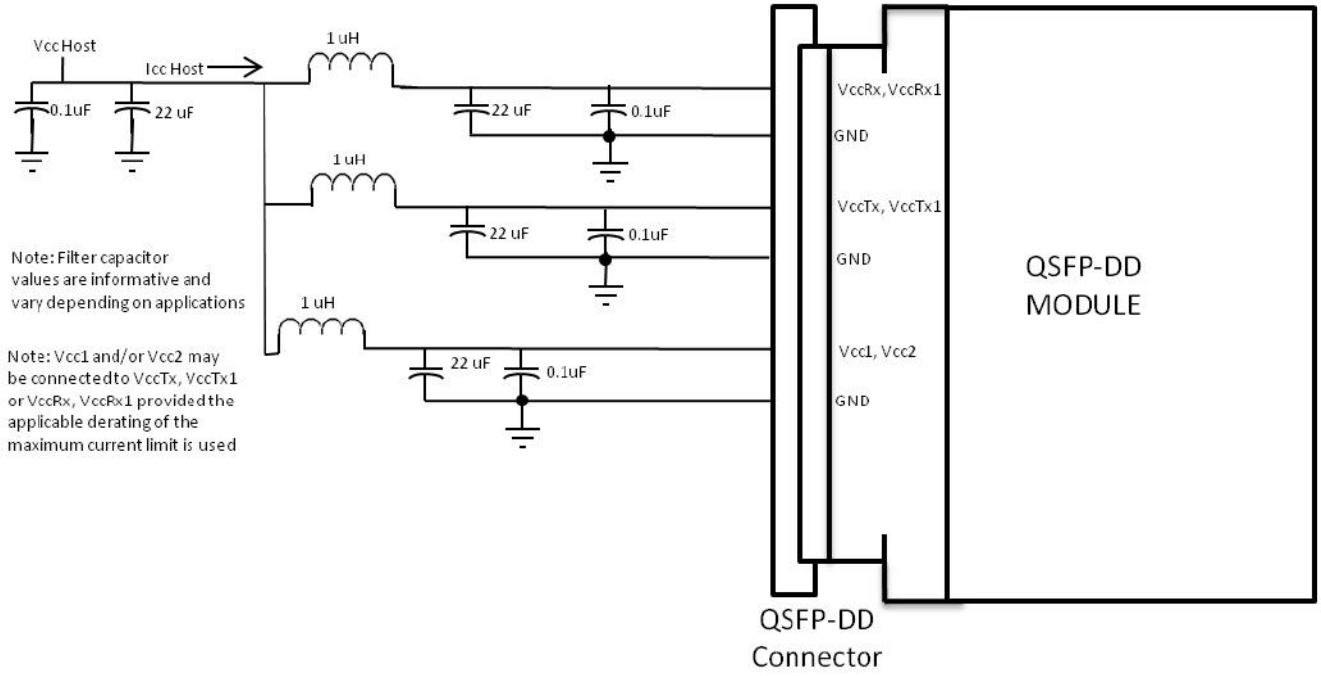


**Figure3. Host Board Power Supply Filtering**

## DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics monitoring function is available on all Gigalight QSFP DD products. A 2-wire serial interface provides user to contact with module.

### Memory Structure and Mapping

This limits the management memory that can be directly accessed by the host to 256 bytes, which is divided in Lower Memory (addresses 00h through 7Fh) and Upper Memory (addresses 80h through FFh).

A larger addressable management memory is required for all but the most basic modules. This is supported by a structure of 128-byte pages, together with a mechanism for dynamically mapping any of the 128-byte pages from a larger internal management memory space into Upper Memory the host addressable space.

The addressing structure of the additional internal management memory is shown in Figure 4 The management memory inside the module is arranged as a unique and always host accessible address space of 128 bytes (Lower Memory) and as multiple upper address subspaces of 128 bytes each (Pages), only one of which is selected as host visible in Upper Memory. A second level of Page selection is possible for Pages for which several instances exist (e.g. where a bank of pages with the same Page

number exists).

This structure supports a flat 256 byte memory for passive copper modules and permits timely access to addresses in the Lower Memory, e.g. Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function in the Lower Page. For more complex modules which require a larger amount of management memory the host needs to use dynamic mapping of the various Pages into the host addressable Upper Memory address space, whenever needed.

**Note**: The management memory map has been designed largely after the QSFP memory map. This memory map has been changed in order to accommodate 8 electrical lanes and to limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

### Supported Pages

A basic 256 byte subset of the Management Memory Map is mandatory for all CMIS compliant devices. Other parts are only available for paged memory modules, or when advertised by the module. See CMIS V4.0 for details regarding the advertisement of supported management memory spaces.

In particular, support of the Lower Memory and of Page 00h is required for all modules, including passive copper cables. These pages are therefore always implemented. Additional support for Pages 01h, 02h and bank 0 of Pages 10h and 11h is required for all paged memory modules.

Bank 0 of pages 10h-1Fh, provides lane-specific registers for the first 8 lanes, and each additional bank provides support for additional 8 lanes. Note, however, that the allocation of information over the banks may be page specific and may not to be related to grouping data for 8 lanes.

The structure allows address space expansion for certain types of modules by allocating additional Pages. Moreover, additional banks of pages.

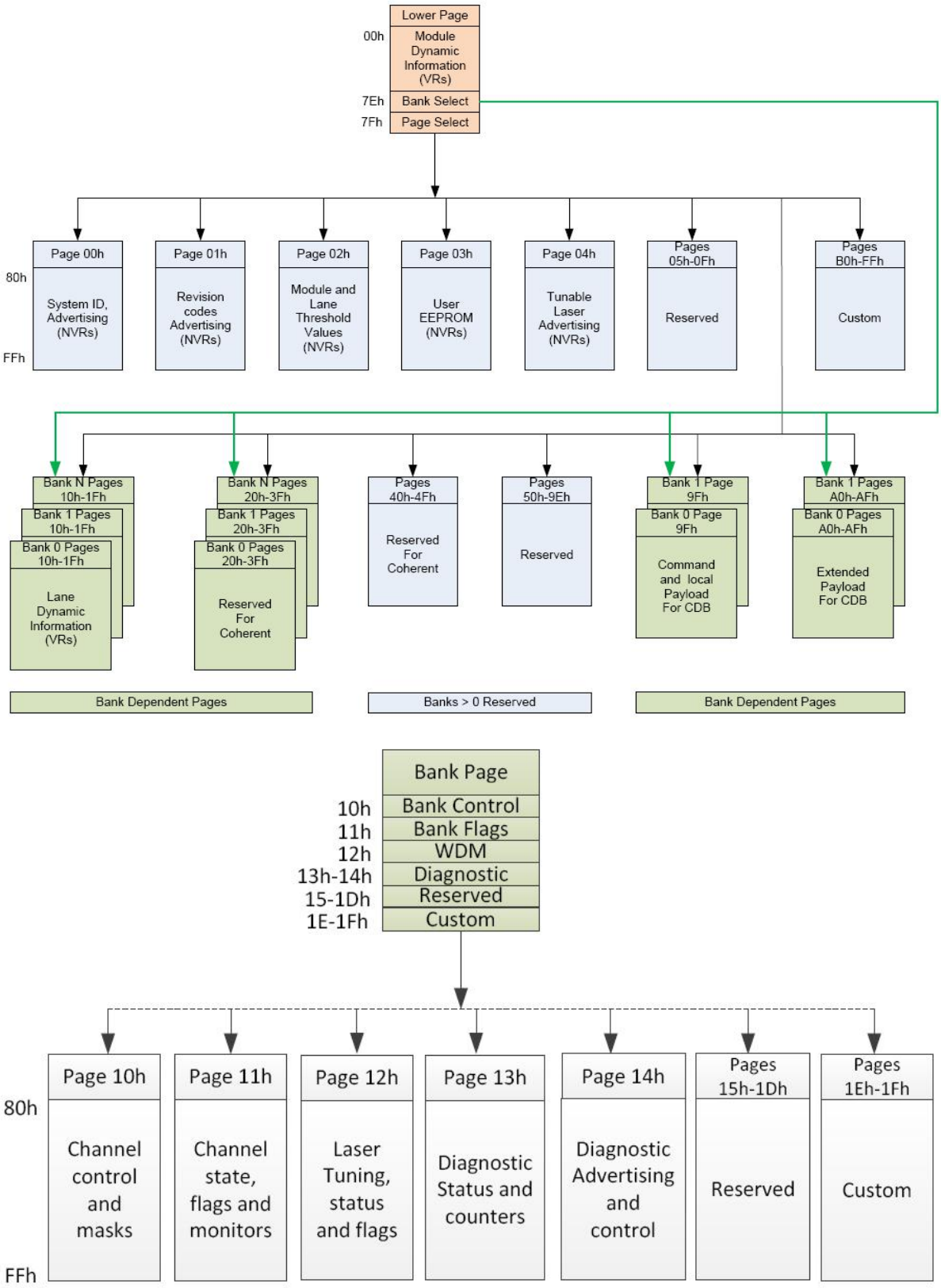


**Figure4. QSFP DD Memory Map**

## Mechanical Dimensions(mm)

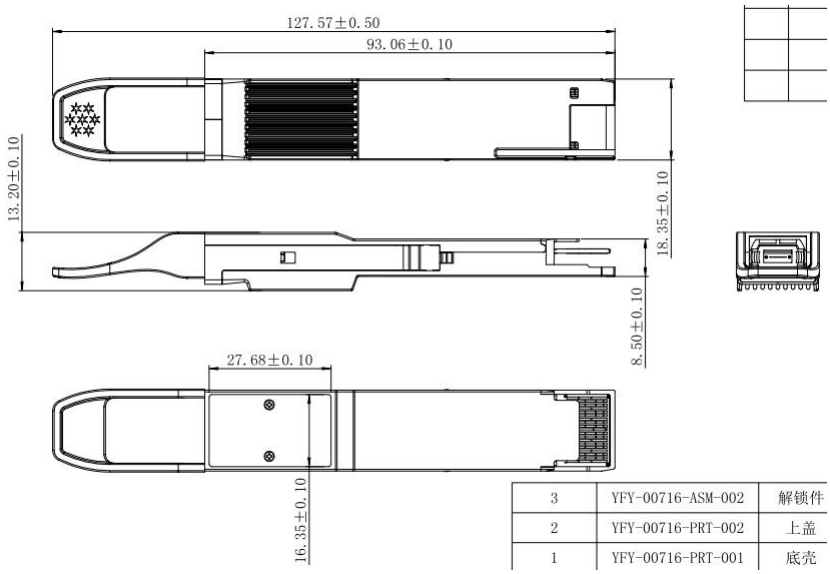


**Figure5. Mechanical Specifications**

## Regulatory Compliance

Gigalight GQD-SI801DR8C transceivers are Class 1 Laser Products. They meet the requirements of the following standards：

| Feature | Standard |
|---|---|
| Laser Safety | IEC 60825-1:2014 (3rd Edition)<br>IEC 60825-2:2004/AMD2:2010<br>EN 60825-1-2014<br>EN 60825-2:2004+A1+A2 |
| Electrical Safety | EN 62368-1: 2014<br>IEC 62368-1:2014<br>UL 62368-1:2014 |
| Environmental protection | Directive 2011/65/EU with amendment(EU)2015/863 |
| CE EMC | EN55032：2015<br>EN55035：2017<br>EN61000-3-2:2014<br>EN61000-3-3:2013 |
| FCC | FCC Part 15, Subpart B<br>ANSI C63.4-2014 |

## References

1. QSFP-DD MSA

2. CMIS
3. IEEE802.3
4. OIF CEI-112G-VSR

**⚠CAUTION:**

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

## Ordering information

| Part Number | Product Description |
|---|---|
| GQD-SI801DR8C | QSFPDD, 800GBASE-DR8, 500m on Single mode Fiber (SMF),with DSP MPO-16 connector. |

## Important Notice

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## Revision History

| Revision | Date | Description |
|---|---|---|
| V0 | Sep-25-2023 | Advance Release. |
| V1 | Oct-12-2023 | Updated structure pull ring color |