

QSFP+ Direct Attach Passive Copper Cable GQS-PC560-XXXXC

Features

- ◆ QSFP+ conforms to the Small Form Factor SFF-8436
- ◆ 4-Channel Full-Duplex Passive Copper Cable Transceiver
- ◆ Low Insertion Loss
- ◆ Maximum aggregate data rate: 56 Gb/s (4 x 14.02Gb/s)
- ◆ Copper link length up to 5m (passive limiting)
- ◆ High-Density QSFP 38-PIN Connector
- ◆ Power Supply :+3.3V
- ◆ Low power consumption: 0.02 W (typ.)
- ◆ I2C based two-wire serial interface for EEPROM signature which can be customized (MCU Optional)



Applications

InfiniBand4x FDR

STANDARDS COMPLIANCE

- ◆ IEEE 802.3ba
- ◆ SFF-8436
- ◆ InfiniBand FDR
- ◆ RoHS Compliant

Product Description

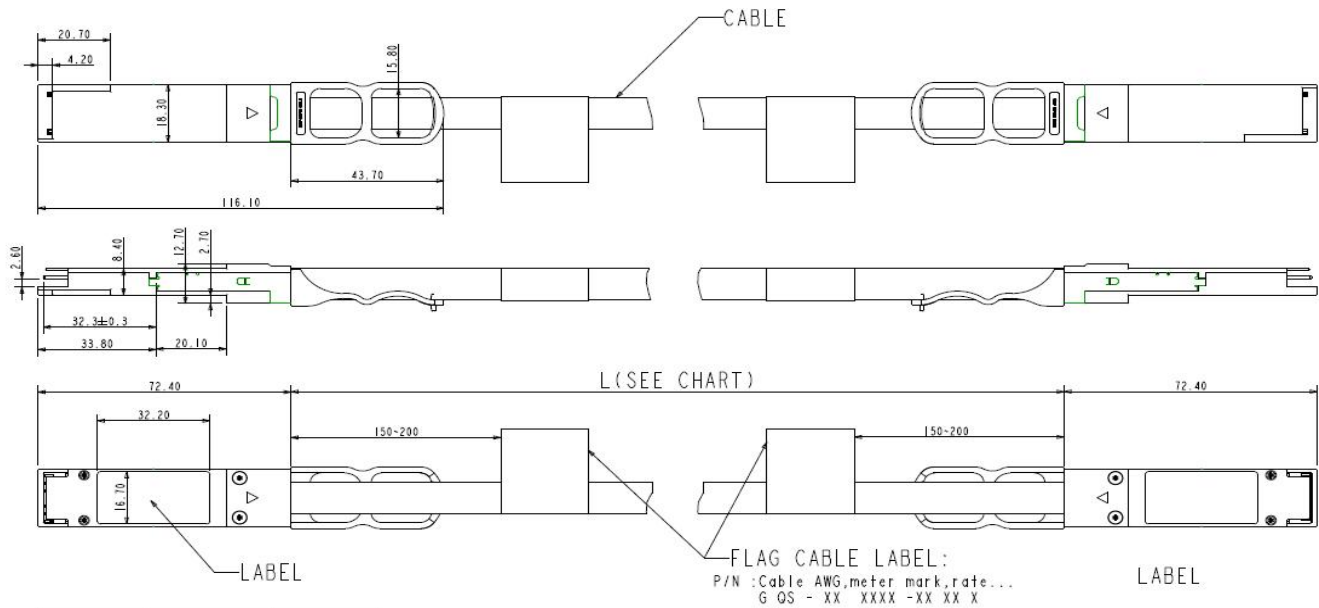
The QSFP+ passive cable assemblies are high performance, cost effective I/O solutions for 56G LAN, HPC and SAN applications. The QSFP+ passive copper cables are compliant with SFF-8436 and

InfiniBand FDR. It is offer a low power consumption, short reach interconnect applications. The cable each lane is capable of transmitting data at rates up to 14 Gb/s, providing an aggregated rate of 40Gb/s.

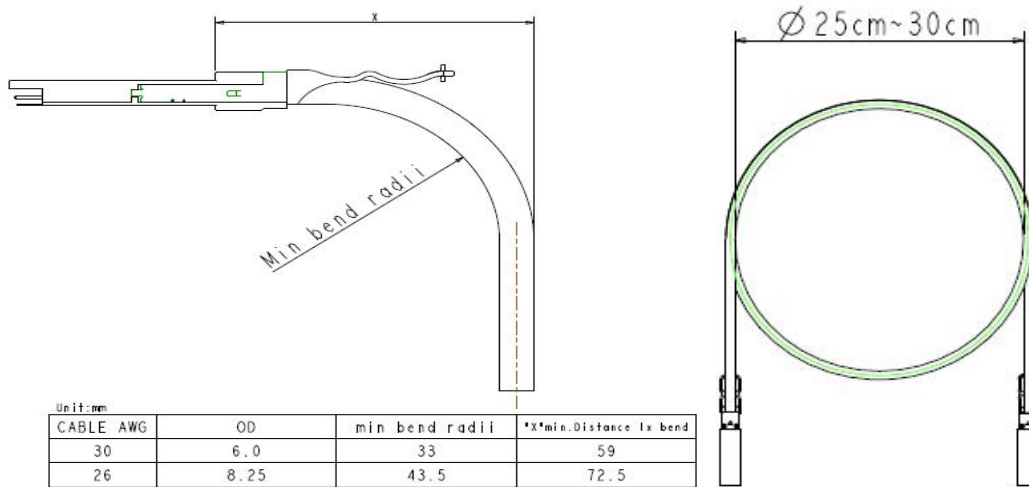
Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Storage Ambient Temperature		-40		+85	°C
Operating Case Temperature	T _c	0		+70	°C
Power Supply Voltage	V _{CC3}	3.14	3.3	3.47	V
Power Dissipation	PD			0.02	W

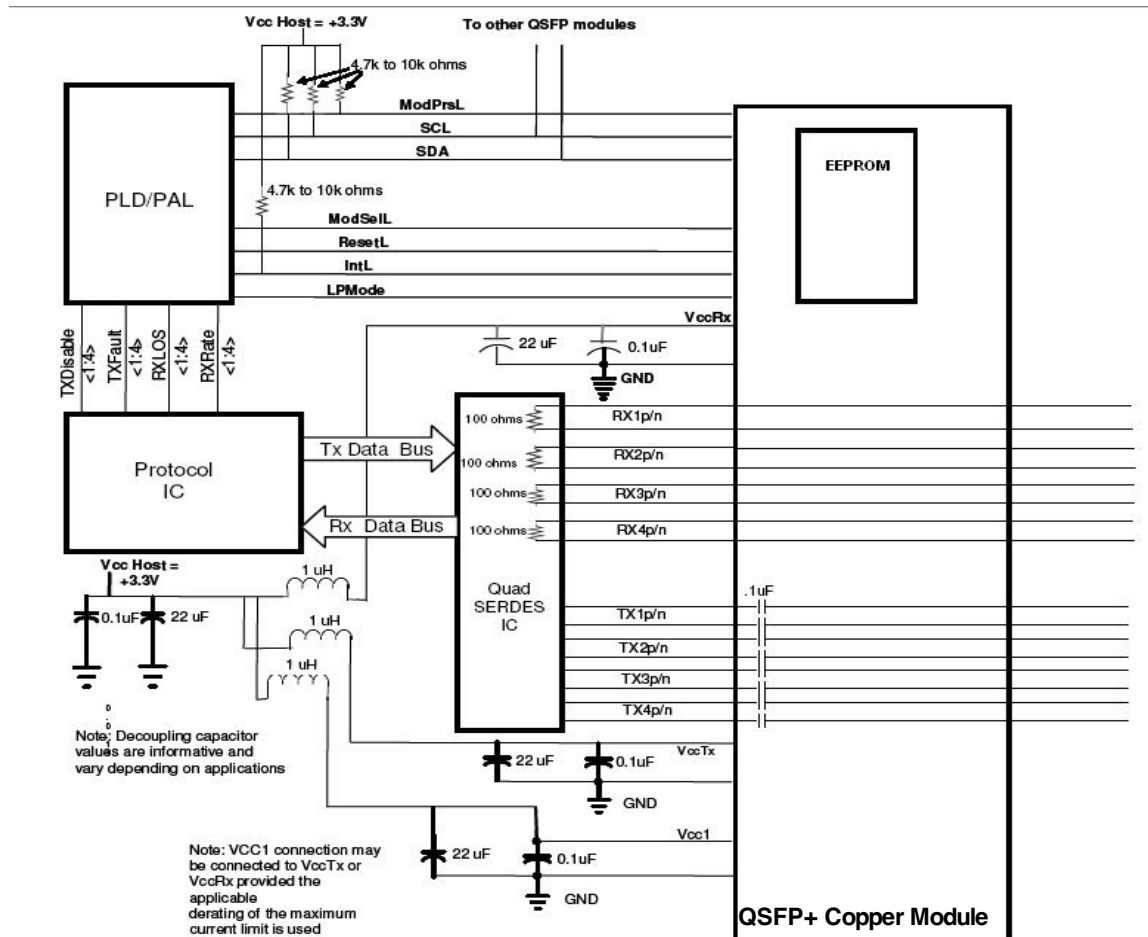
Mechanical Dimensions



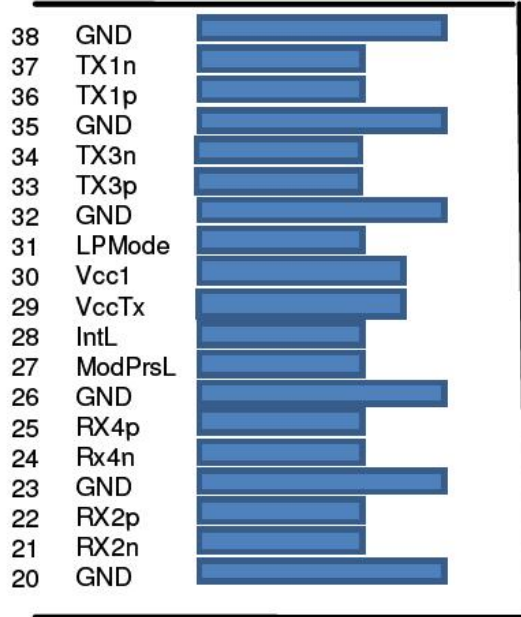
代码	长度范围 (m)	公差 (cm)
L	L ≤ 0.5	±3
	0.5 < L ≤ 5	±5
	5 < L ≤ 20	±8
	20 < L	±10



QSFP+ Host Board Schematic for passive copper cables

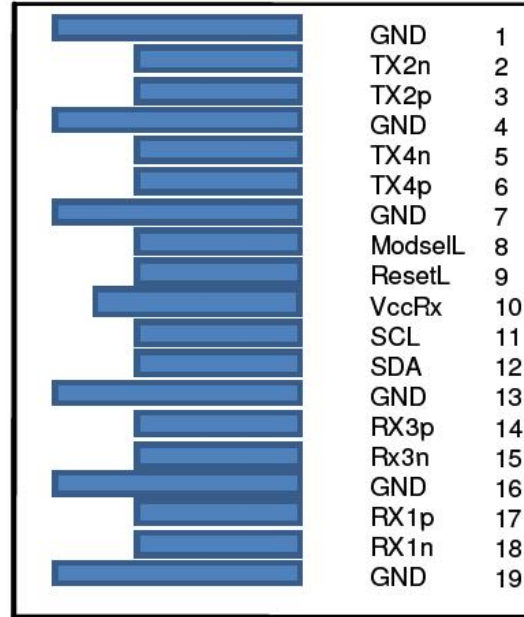


Pin Descriptions



Top Side
Viewed From Top

Module Card Edge



Bottom Side
Viewed From Bottom

Pin	Logic	Symbol	Name/Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		Vcc Rx	+3.3V Power Supply Receiver	2
11	LVCMOSI/O	SCL	2-wire serial interface clock	
12	LVCMOSI/O	SDA	2-wire serial interface data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	

16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		Vcc Tx	+3.3V Power supply transmitter	2
30		Vcc1	+3.3V Power supply	2
31	LVTTL-I	LPMODE	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1

Note 1: GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table 6. Recommended host board power supply filtering is shown in Figure 4. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ Module module in any combination. The connector pins are each rated for a maximum current of 500 mA.



Ordering information

Part Number	GQS-PC560-XXXXC				
Length (meter)	1	2	3	4	5
Wire gauge (AWG)	30	30	28	26	26

Important Notice

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